

# Compal Confidential

## DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2012-08-06

[www.rosefix.com](http://www.rosefix.com)

REV: 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title		
				Cover Page		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT OF DEFENSE TO ANY OTHER PERSON OR ENTITY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9641P	Rev
				Date	Thursday, October 11, 2012	Sheet 1 of 60

# Shark Bay

**AMD MARS XT M2 128 bits  
/ SUN PRO M2 64 bits**

VRAM 512MB/1GB/2GB  
MARS XT : DDR3 x 8  
SUN PRO : DDR3 x 4

page 23~32

PEG 8x  
Gen2 / Gen3

**Intel  
Processor  
Haswell**

rPGA946  
37.5mm x 37.5mm

page 5,~11

Memory Bus  
Dual Channel

DDR3L 1600MHz  
DDR3L 1333MHz

**204pin DDRIII-SO-DIMM X2**

BANK 0, 1, 2 page 12,13

**LVDS Conn.**  
page 31

**LVDS Translator**  
RTD2132R(Single)  
page 33

**HDMI Conn.**  
page 36

FDI \*2  
2.7GT/s

DMI2 \*4  
5GT/s

**Intel  
PCH  
Lynx Point**

FCBGA 695Balls  
20mm x 20mm

USB30 x2

USB20 x6

**Left USB3.0 x2**  
USB30 Port 0,1  
page 46

**Right USB2.0**  
USB20 Port 9  
page 46

**Int. Camera**  
USB20 Port 3  
page 33

**Touch Screen**  
USB20 Port 2

**Card Reader**  
Realtek RTS5170  
USB20 Port 11  
page 44

**CRT Conn.**  
page 35

**RJ45 Conn.**  
page 39

**LAN**  
Atheros  
AR8162/QCA8172 (10/100)  
page 38

PCIe x1

**PCIe Mini Card**  
**WiMax**  
USB20 Port 10  
page 28

PCIe x1

**PCIe Mini Card**  
**WLAN**  
PCIe Port 0  
page 28

USB20 x1

SATA Gen3

**HDD Conn.**  
SATA Port 4  
page 41

SATA

**ODD Conn.**  
SATA Port 5  
page 41

AZALIA

**Audio Codec**  
CONEXANT  
CX20757  
page 42

**Int. MIC Conn.**  
page 42

**Int. Speaker Conn.**  
page 42

**Audio Combo Jacks**  
HP & MIC  
page 42

Sub-board

15"

**ODD/B**  
LSXXXP  
page 44

14"

**Power/B**  
LSXXXP  
page 44

**LED/B**  
LSXXXP  
page 44

**USB/B**  
LSXXXP  
page 44

**CR/B**  
LSXXXP  
page 44

**SPI ROM**  
2MB + 4MB  
page 17

**EC**  
ENE KB9012  
page 44

**Thermal Sensor**  
page 40

**Touch Pad**  
page 44

**Int. KBD**  
page 44

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT TO ANY OTHER DEPARTMENT OR TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-9641P	2.0
				Date: Thursday, October 11, 2012	Sheet 2 of 60

Voltage Rails				
power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS
				+VCC_CORE +VGA_CORE
State				+1.5VS +0.675VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor	1001_100xb

### PCH SM Bus address

### AMD-GPU SM Bus address

Device	Address	Device	Address
DDR DIMM0	1001 000Xb	Internal thermal sensor	1000_001xb
DDR DIMM2	1001 010Xb		

Device	Address
RTD2132R	1101 010Xb

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	X	X
SMB_EC_DA2	+3VALW							+3VS	+3VS
SMBCLK	PCH	X	X	X	V	V	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	V	X	V	X	X	V	X	V
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%	Board ID / SKU ID Table for AD channel				
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

### USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
7			
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
	UHCI6	12	
		13	

### BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Cameara	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
GREEN CLOCK	GCLK@
DIS GREEN CLOCK	GCLK304@
UMA GREEN CLOCK	GCLK244@
NO GREEN CLOCK	NOGCLK@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

VRAM BOM STRUCTURE Refer P4. VGA NOTE

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Notes List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN PERMISSION OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. ANY REPRODUCTION OR DISSEMINATION OF THIS INFORMATION WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. IS STRICTLY PROHIBITED.				Document Number	LA-9641P	Rev 2.0
				Date	Thursday, October 11, 2012	Sheet 3 of 60

## Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

## Mars XT VRAM STRAP

X76@

X76@

	Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@	Hynix 2048Mbits TBD H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC

ZZZ4  
Samsung\_2G  
MS2G@  
X7646738L01

ZZZ5  
Micron\_2G  
MM2G@  
X7646738L02

ZZZ6  
Hynix\_2G  
MH2G@  
TBD

ZZZ7  
Samsung\_1G  
MS1G@  
X7646738L03

ZZZ8  
Hynix\_1G  
MH1G@  
X7646738L04

VDDR3(3.3VGS)

PCIE\_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD\_CT(1.8V)

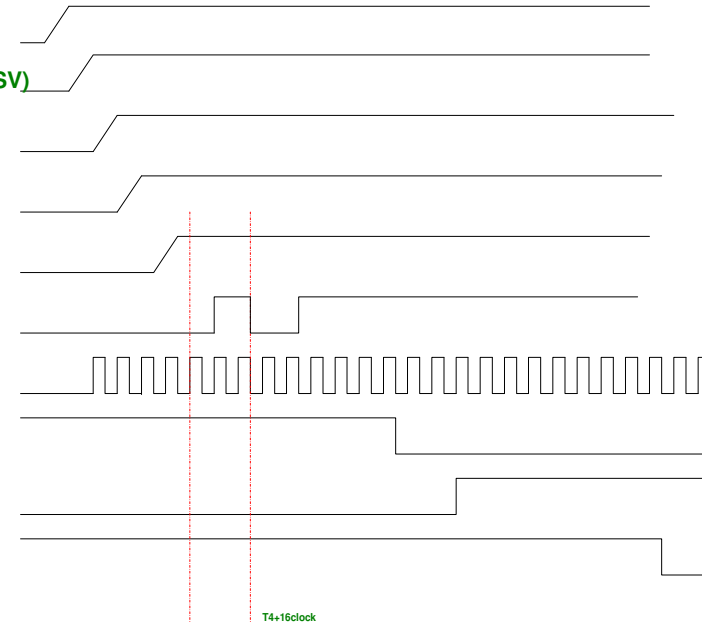
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset



## Sun PRO VRAM STRAP

X76@

X76@

	Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-109G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@	Hynix 2048Mbits TBD H5TQ2G63DFR-N0C	1	1	1	4.75K	NC

ZZZ9  
Samsung\_2G  
SS2G@  
X7646738L05

ZZZ10  
Micron\_2G  
SM2G@  
X7646738L06

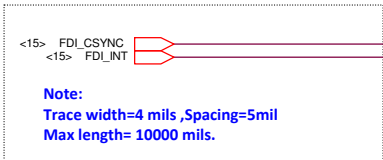
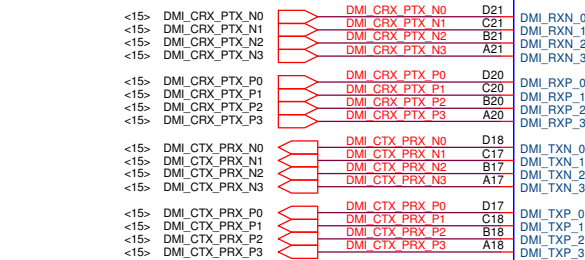
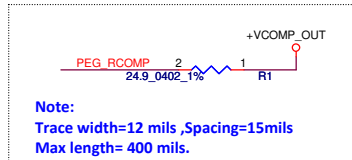
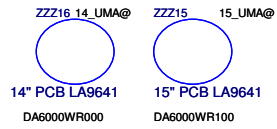
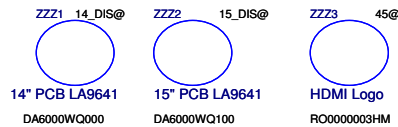
ZZZ11  
Hynix\_2G  
SH2G@  
TBD

ZZZ12  
Samsung\_1G  
SS1G@  
X7646738L07

ZZZ13  
Micron\_1G  
SM1G@  
X7646738L08

ZZZ14  
Hynix\_1G  
SH1G@  
TBD

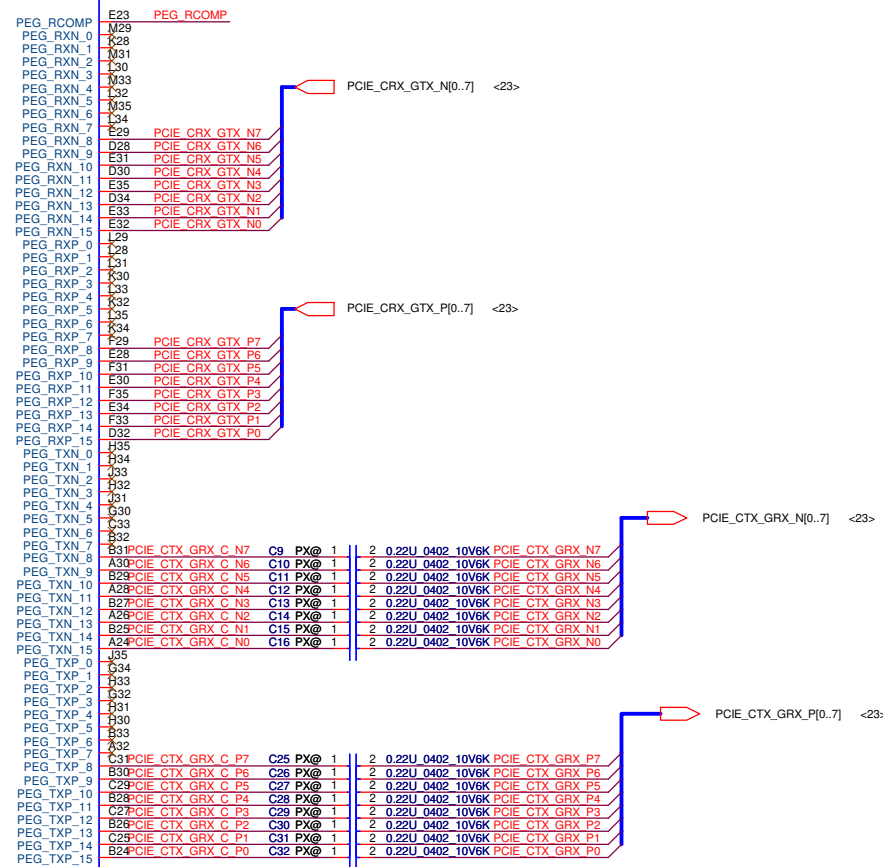
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	VGA Notes List
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE COMPANY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9641P
				Date	Thursday, October 11, 2012
				Sheet	4 of 60



Haswell rPGA EDS  
JCPU1A

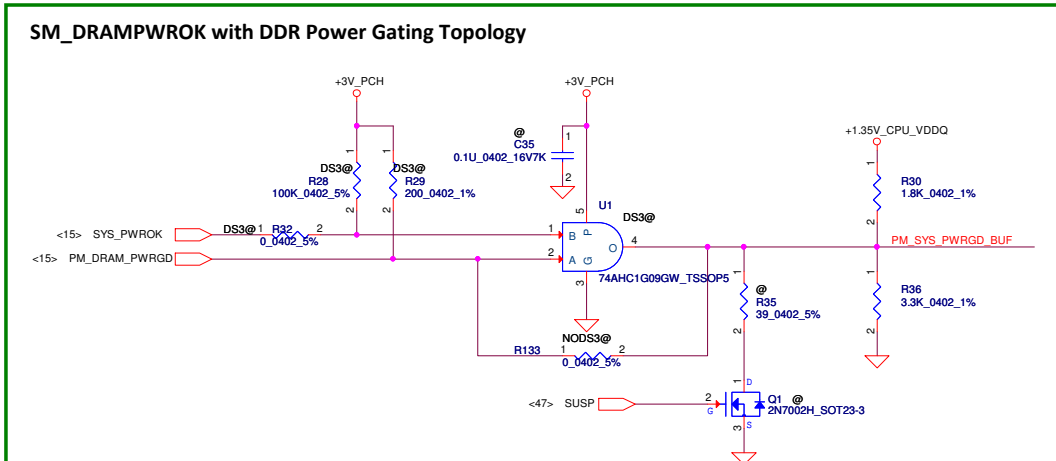
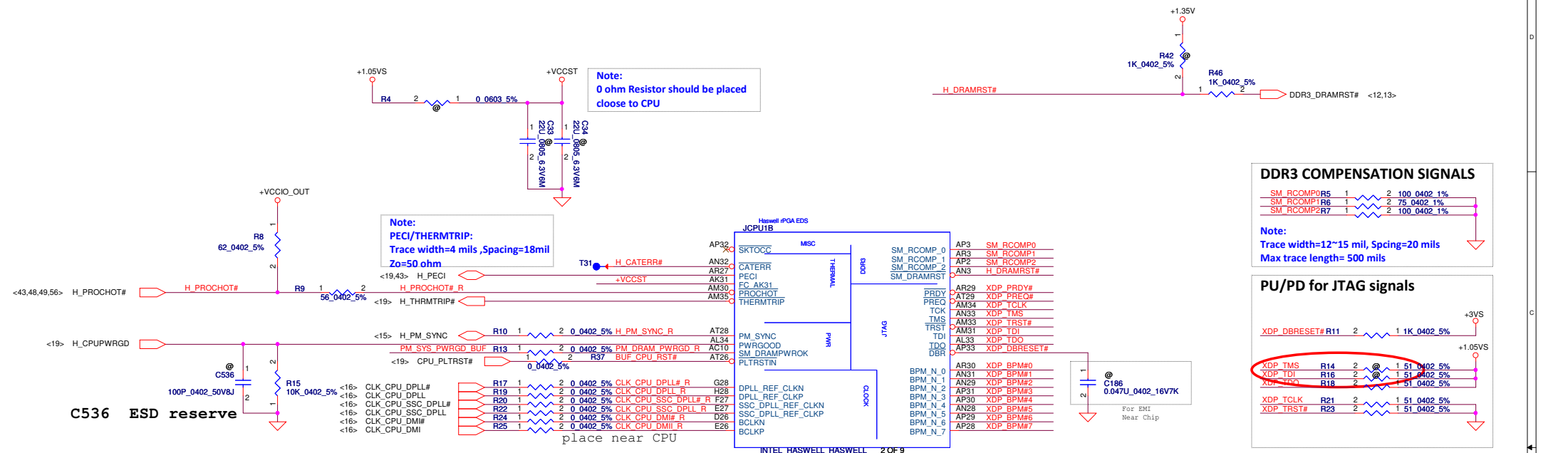


INTEL\_HASWELL\_HASWELL 1 OF 9  
ME@



Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PROCESSOR(1/7) DMI,FDI,PEG	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTOMER TO ANY OTHER PARTY WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 0.1
LA-9641P				Date: Thursday, October 11, 2012	Sheet 5 of 60

www.vinafix.vn



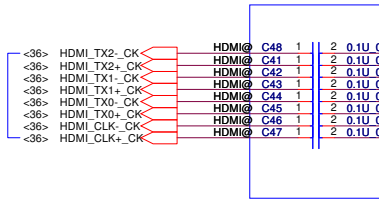
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT OR CUSTOMER. ANY UNAUTHORIZED REPRODUCTION OR DISSEMINATION OF THIS SHEET OR THE INFORMATION IT CONTAINS MAY BE USED TO DISCLOSE TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR(2/7) PM,XDP,CLK	
				Document Number	Rev
				LA-9641P	0.1
				Date: Thursday, October 11, 2012	Sheet 6 of 60

www.vinallix.vn

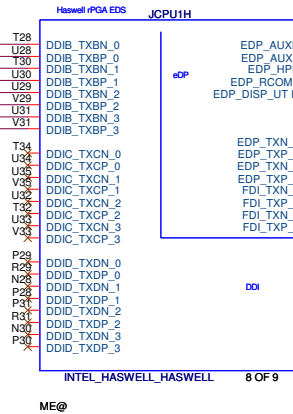


HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

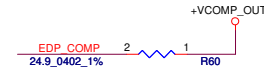
HDMI



Place on connector side

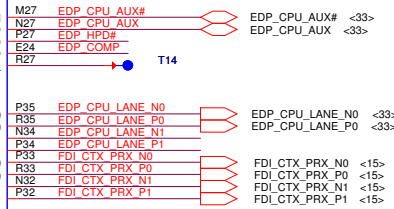


### COMPENSATION PU FOR eDP

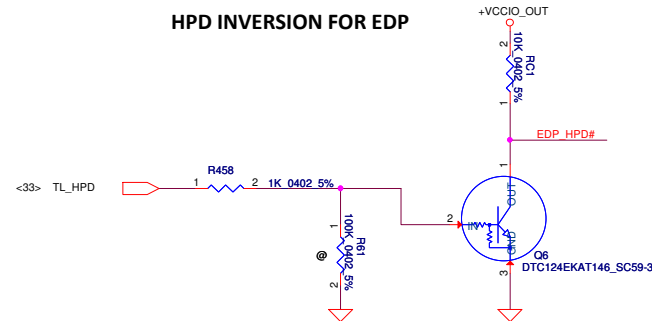


Note:

Trace width=20 mils, Spacing=25mil,  
Max length=100 mils.



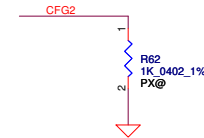
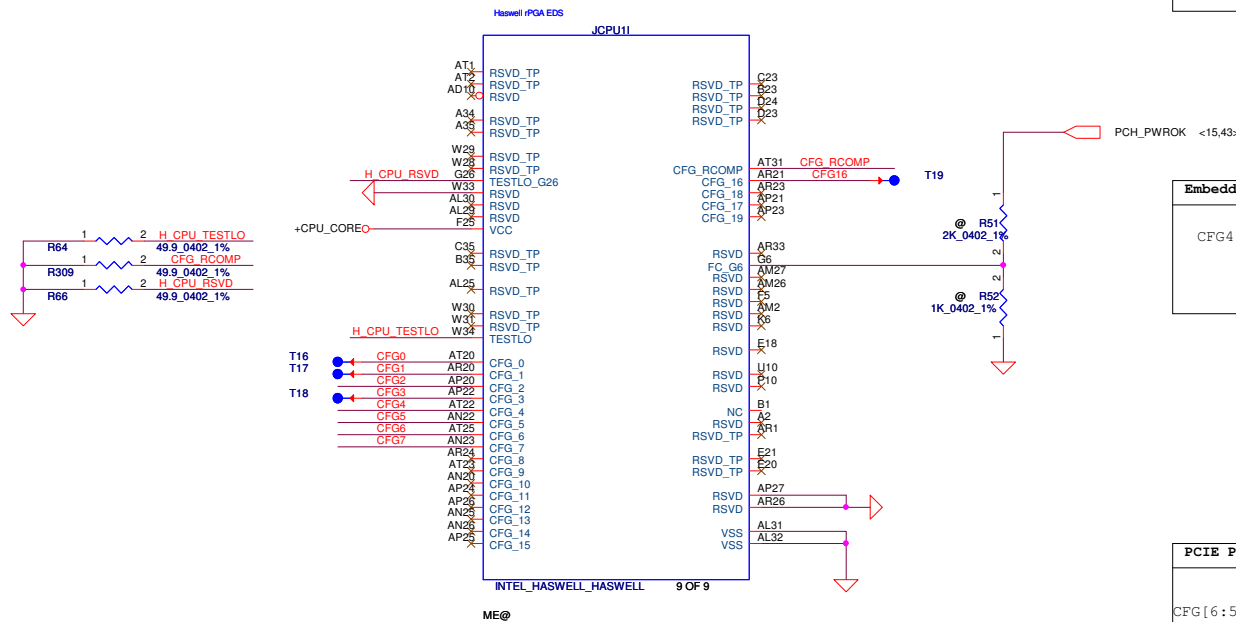
### HPD INVERSION FOR EDP



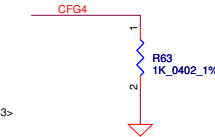
HPD is a active high signal from device. The HPD processor input is a low voltage active signal.



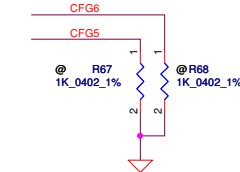
## CFG Straps for Processor



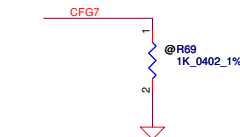
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

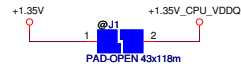


PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



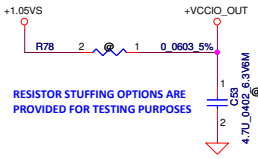
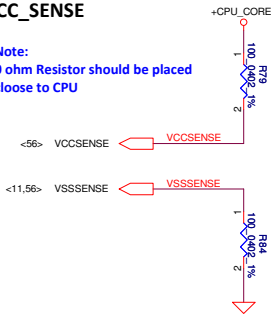
PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

# +1.35V\_CPU\_VDDQ Source

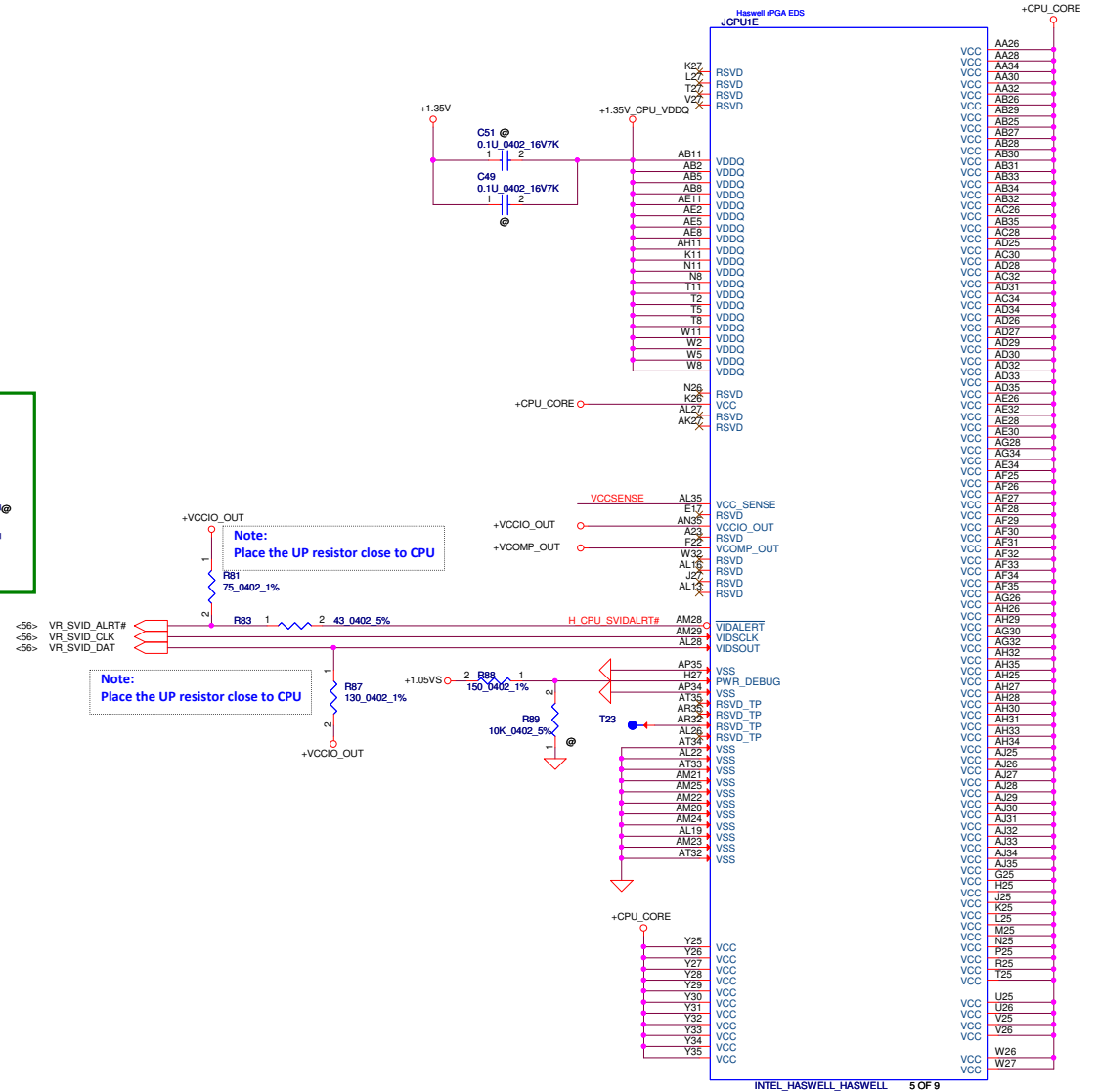
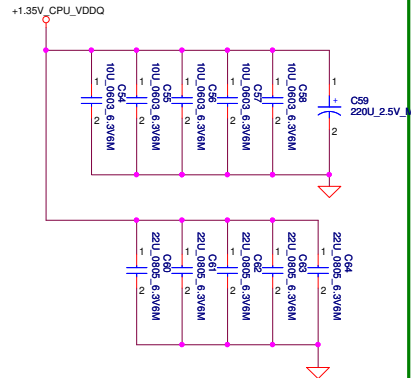


## VCC\_SENSE

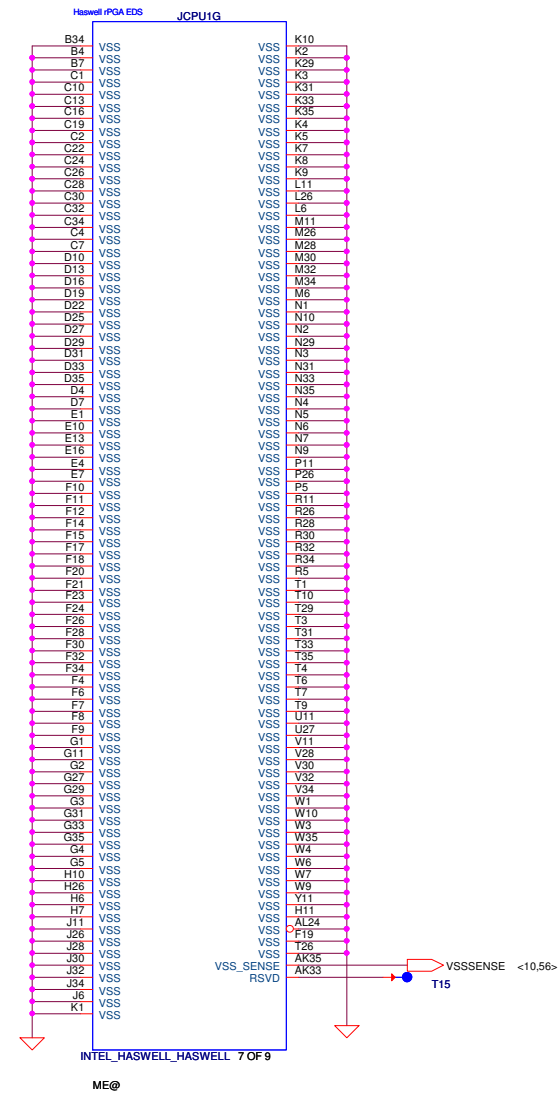
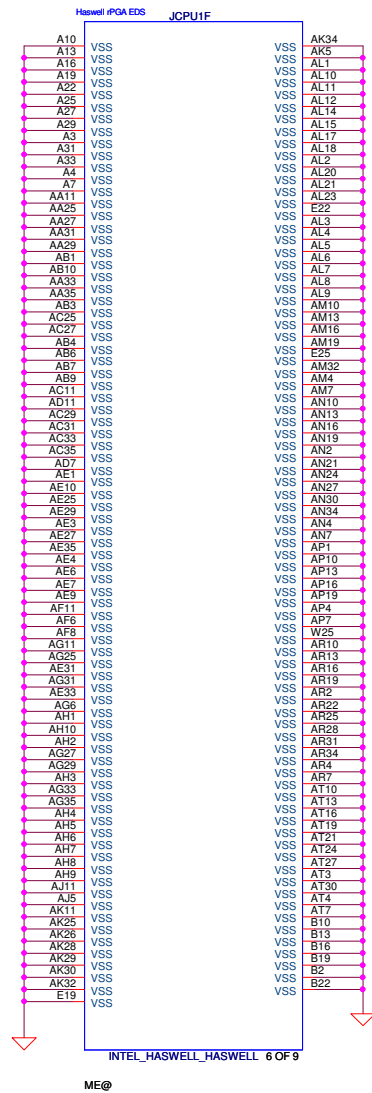
Note:  
0 ohm Resistor should be placed  
close to CPU



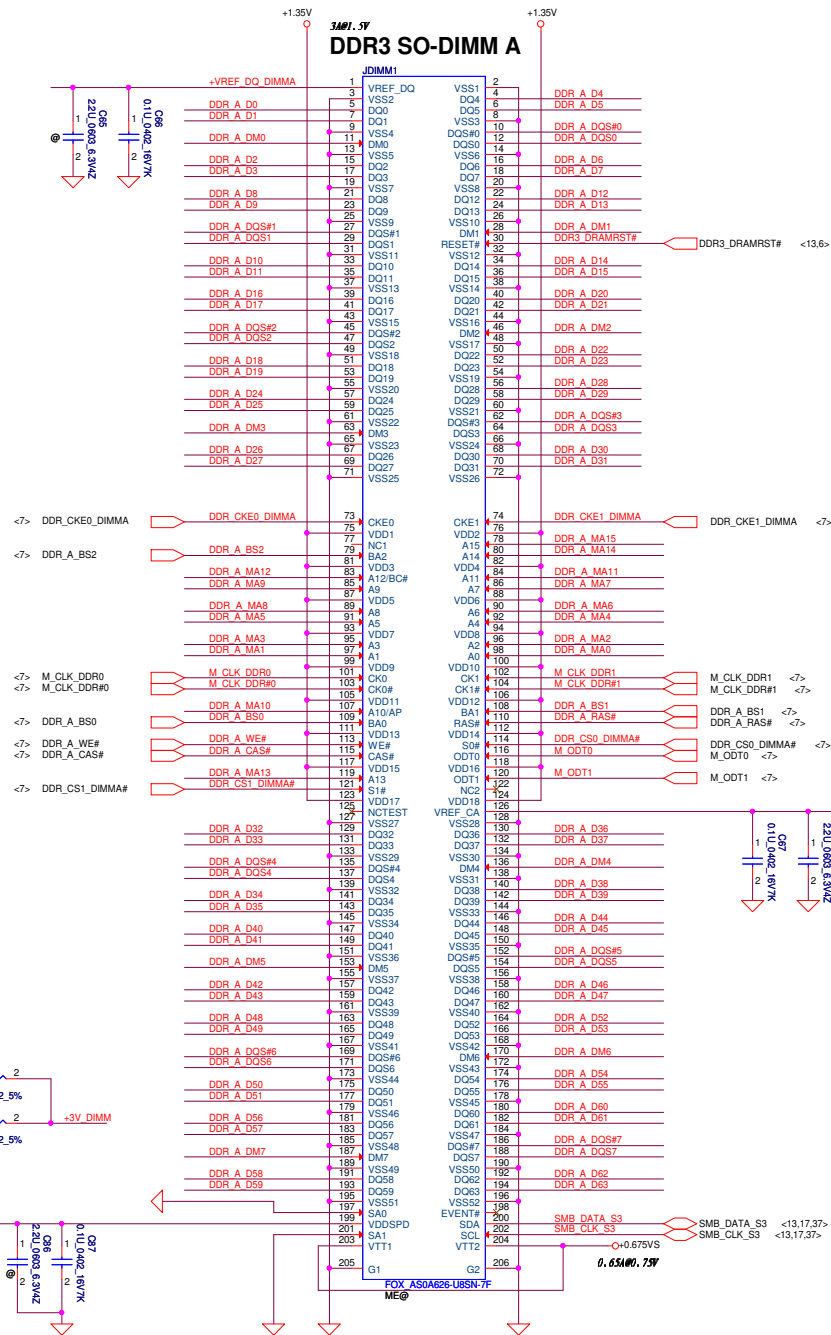
## VDDQ DECOUPLING



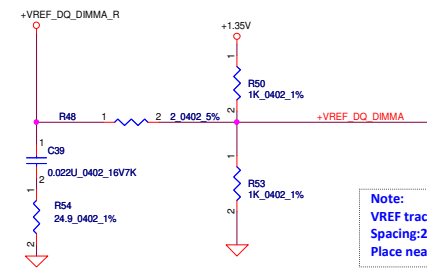
Security Classification	Compal Secret Data			Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PROCESSOR(6/7) PWR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-9641P	0.1
				Date	Thursday, October 11, 2012
				Sheet	10 of 60



# DDR3 SO-DIMM A



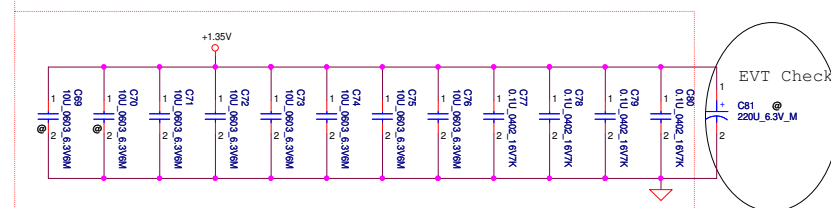
<7> DDR\_A\_D[0..63]  
<7> DDR\_A\_DQS[0..7]  
<7> DDR\_A\_DQS#0..7  
<7> DDR\_A\_MA[0..15]



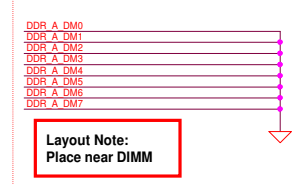
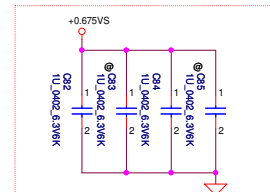
Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes  
Place near DIMM socket

Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes  
Place near DIMM socket

Layout Note:  
Place near DIMM

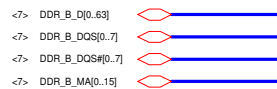


Layout Note:  
Place near DIMM



Layout Note:  
Place near DIMM

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	DDR3-SODIMM SLOT1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 2.0
				Document Number LA-7981P	Sheet 12 of 60
				Date Thursday, October 11, 2012	Sheet 12 of 60



+0.675VS

C104  
1UJ0402 0.3V0K

C105  
1UJ0402 0.3V0K

C106  
1UJ0402 0.3V0K

C107  
1UJ0402 0.3V0K

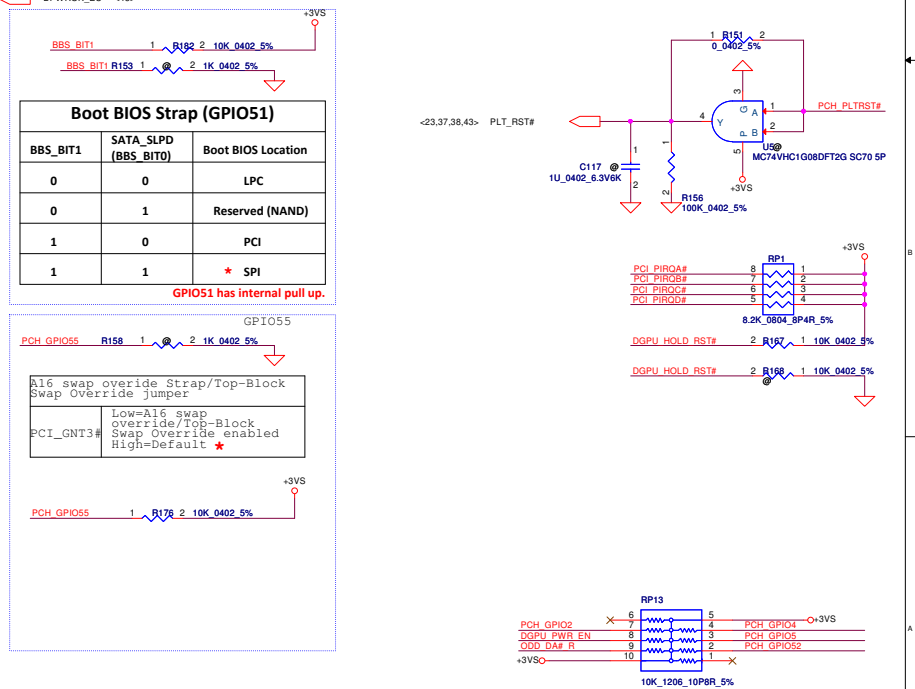
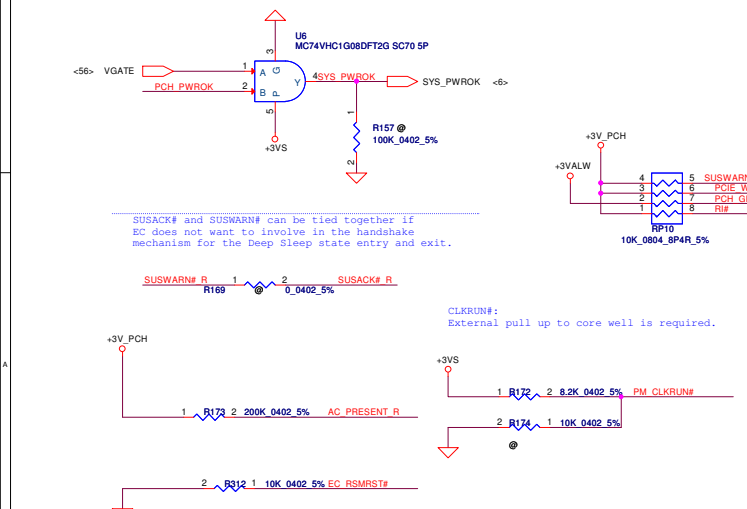
C108  
1UJ0402 0.3V0K

DDR B DM0  
DDR B DM1  
DDR B DM2  
DDR B DM3  
DDR B DM4  
DDR B DM5  
DDR B DM6  
DDR B DM7

**Layout Note:**  
**Place near DIMM**

DDR B DM0	
DDR B DM1	
DDR B DM2	
DDR B DM3	
DDR B DM4	
DDR B DM5	
DDR B DM6	
DDR B DM7	

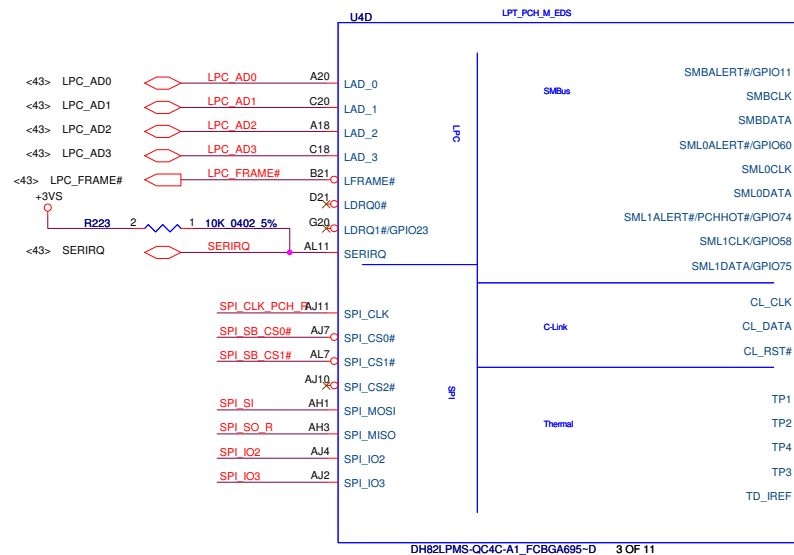




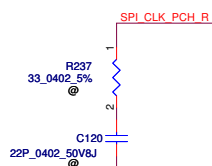
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2011/06/15	Deciphered Date		2012/07/11	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		
				PCH (2/9) PCIE, SMBUS, CLK		
				Size	Document Number	Rev
				LA-9641P		
				Date:	Thursday, October 11, 2012	Sheet 15 of 60



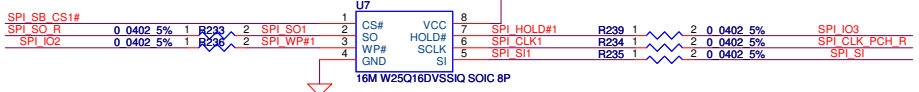
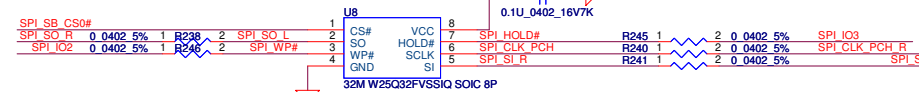




## 8MB SPI ROM FOR ME & Non-share ROM.



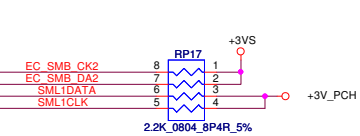
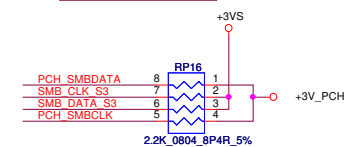
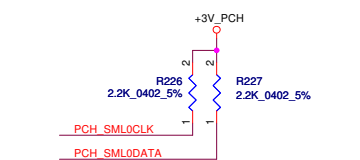
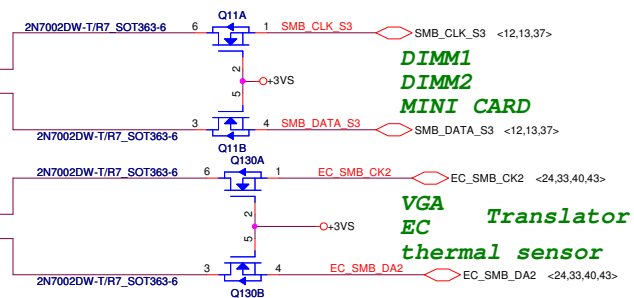
R124;c190 close to U4.T3 pin



U7 Rersver 4M+2M Solution

PCH\_SMBCLK R190 1 2 0 0402\_5% SMB\_CLK S3

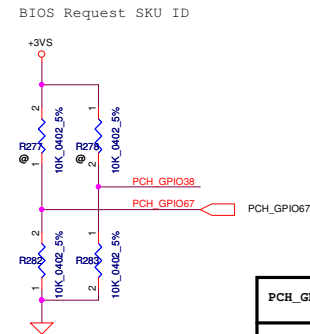
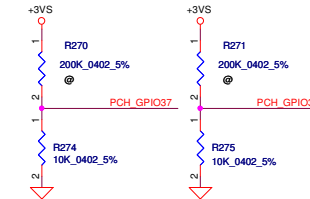
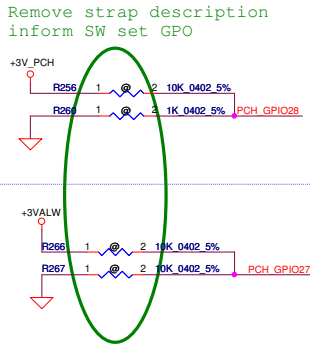
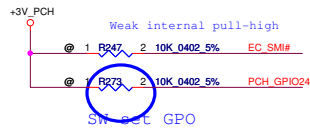
PCH\_SMBDATA R200 1 2 0 0402\_5% SMB\_DATA S3



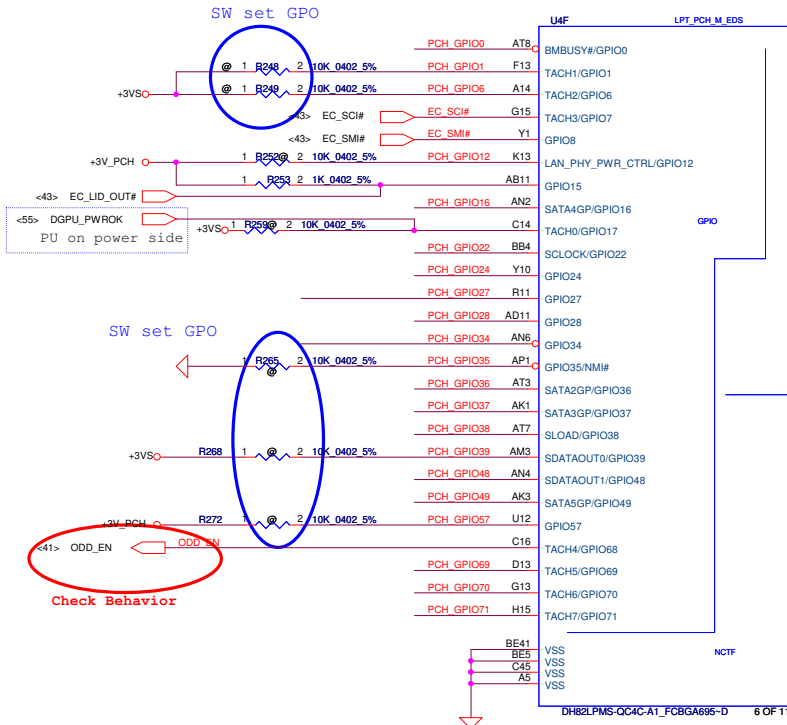
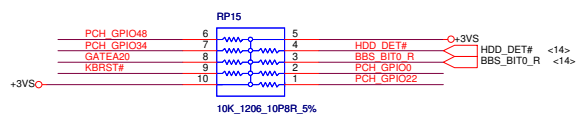
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2011/06/15		Deciphered Date		2012/07/11	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HEAD DEPARTMENT OR BE LOANED, REPRODUCED, COPIED, OR DISCLOSED TO ANY OTHER PERSON WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title			
				PCH (4/9) LVDS,CRT,DP,HDMI			
				Document Number			
				LA-9641P		Rev 0.1	
				Date:		Thursday, October 11, 2012	
				Sheet		17 of 60	

www.vinallix.vn

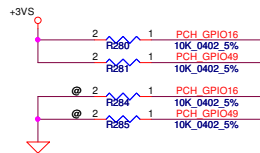




PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	UMA
1	1	DIS

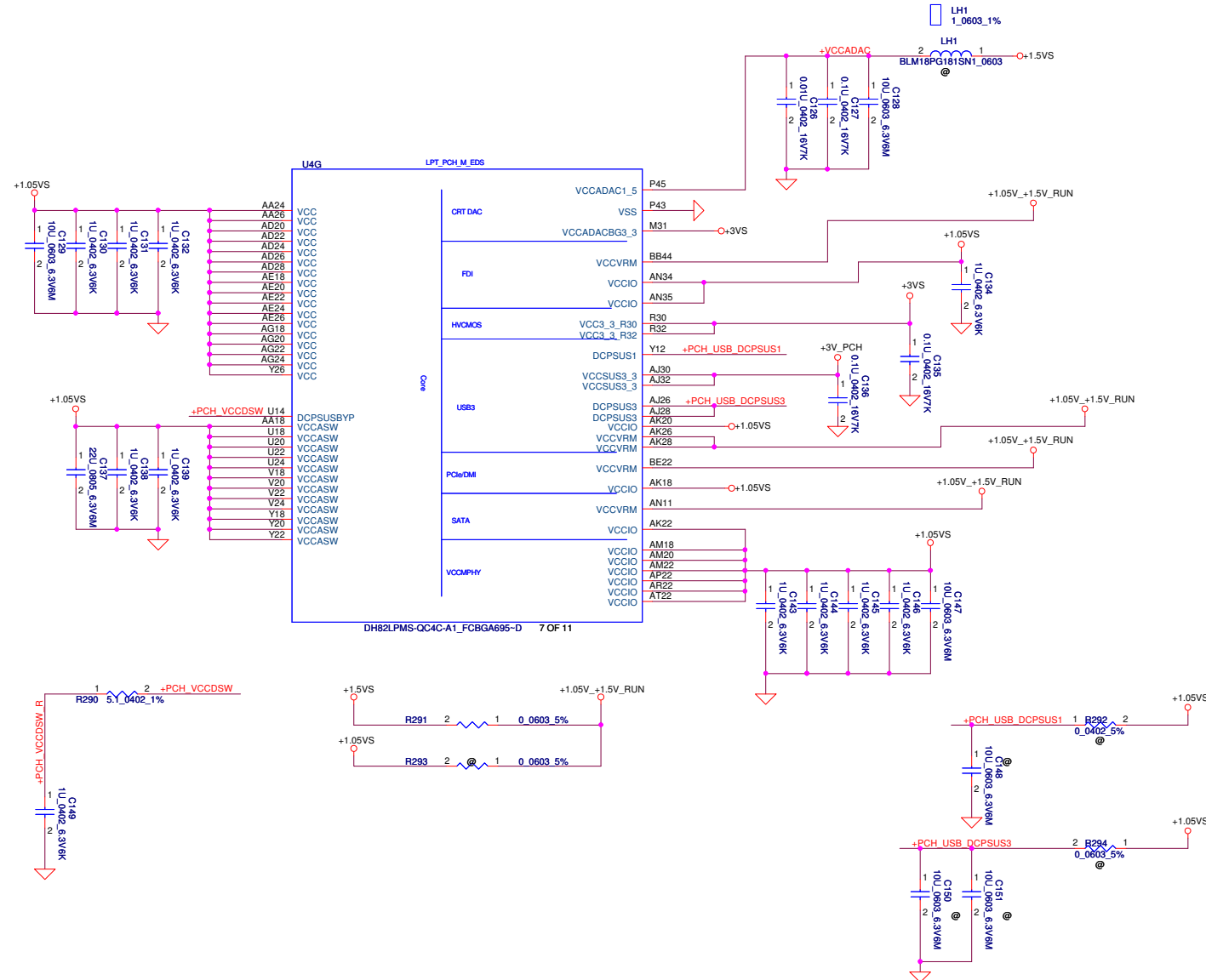


Check Behavior

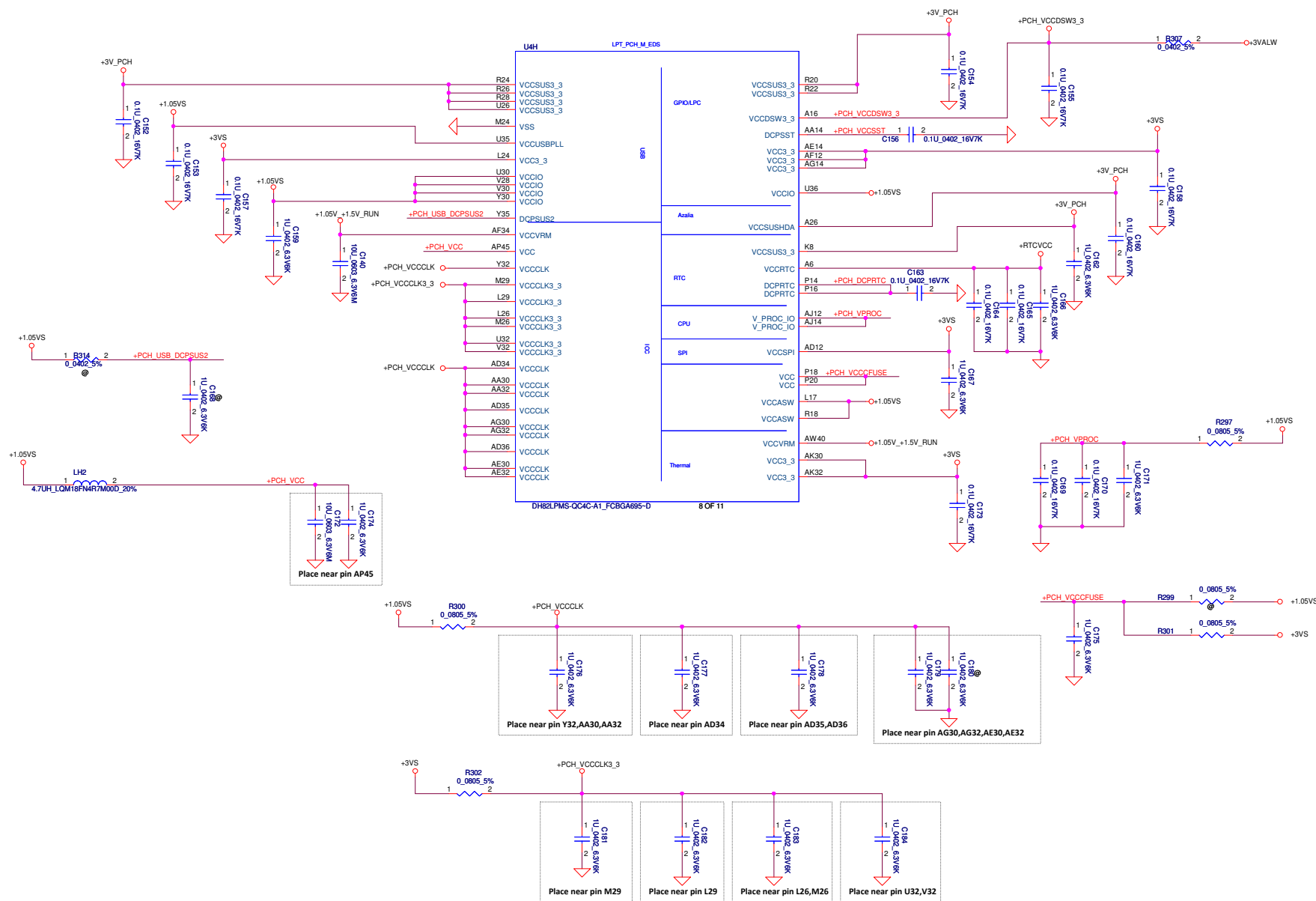


Config	GPIO16 & 49
USB3.0 x4, PCIe x8, SATA x6	11
USB3.0 x6, PCIe x8, SATA x4	01

Fixed Signals	Muxed Signals	Fixed Signals	Muxed Signals	Fixed Signals
USB3 1	PCIe 1	PCIe 3	SATA 1	SATA 1
USB3 2	PCIe 2	PCIe 4	SATA 2	SATA 2
USB3 5	PCIe 3	PCIe 5	SATA 3	SATA 3
USB3 6	PCIe 4	PCIe 6	SATA 4	SATA 4
	PCIe 5	PCIe 7	SATA 5	SATA 5
	PCIe 6	PCIe 8	SATA 6	SATA 6
	PCIe 7	PCIe 9	SATA 7	SATA 7
	PCIe 8	PCIe 10	SATA 8	SATA 8
	PCIe 9	PCIe 11	SATA 9	SATA 9
	PCIe 10	PCIe 12	SATA 10	SATA 10
	PCIe 11	PCIe 13	SATA 11	SATA 11
	PCIe 12	PCIe 14	SATA 12	SATA 12
	PCIe 13	PCIe 15	SATA 13	SATA 13
	PCIe 14	PCIe 16	SATA 14	SATA 14
	PCIe 15	PCIe 17	SATA 15	SATA 15
	PCIe 16	PCIe 18	SATA 16	SATA 16
	PCIe 17	PCIe 19	SATA 17	SATA 17
	PCIe 18	PCIe 20	SATA 18	SATA 18
	PCIe 19	PCIe 21	SATA 19	SATA 19
	PCIe 20	PCIe 22	SATA 20	SATA 20
	PCIe 21	PCIe 23	SATA 21	SATA 21
	PCIe 22	PCIe 24	SATA 22	SATA 22
	PCIe 23	PCIe 25	SATA 23	SATA 23
	PCIe 24	PCIe 26	SATA 24	SATA 24
	PCIe 25	PCIe 27	SATA 25	SATA 25
	PCIe 26	PCIe 28	SATA 26	SATA 26
	PCIe 27	PCIe 29	SATA 27	SATA 27
	PCIe 28	PCIe 30	SATA 28	SATA 28
	PCIe 29	PCIe 31	SATA 29	SATA 29
	PCIe 30	PCIe 32	SATA 30	SATA 30
	PCIe 31	PCIe 33	SATA 31	SATA 31
	PCIe 32	PCIe 34	SATA 32	SATA 32
	PCIe 33	PCIe 35	SATA 33	SATA 33
	PCIe 34	PCIe 36	SATA 34	SATA 34
	PCIe 35	PCIe 37	SATA 35	SATA 35
	PCIe 36	PCIe 38	SATA 36	SATA 36
	PCIe 37	PCIe 39	SATA 37	SATA 37
	PCIe 38	PCIe 40	SATA 38	SATA 38
	PCIe 39	PCIe 41	SATA 39	SATA 39
	PCIe 40	PCIe 42	SATA 40	SATA 40
	PCIe 41	PCIe 43	SATA 41	SATA 41
	PCIe 42	PCIe 44	SATA 42	SATA 42
	PCIe 43	PCIe 45	SATA 43	SATA 43
	PCIe 44	PCIe 46	SATA 44	SATA 44
	PCIe 45	PCIe 47	SATA 45	SATA 45
	PCIe 46	PCIe 48	SATA 46	SATA 46
	PCIe 47	PCIe 49	SATA 47	SATA 47
	PCIe 48	PCIe 50	SATA 48	SATA 48
	PCIe 49	PCIe 51	SATA 49	SATA 49
	PCIe 50	PCIe 52	SATA 50	SATA 50
	PCIe 51	PCIe 53	SATA 51	SATA 51
	PCIe 52	PCIe 54	SATA 52	SATA 52
	PCIe 53	PCIe 55	SATA 53	SATA 53
	PCIe 54	PCIe 56	SATA 54	SATA 54
	PCIe 55	PCIe 57	SATA 55	SATA 55
	PCIe 56	PCIe 58	SATA 56	SATA 56
	PCIe 57	PCIe 59	SATA 57	SATA 57
	PCIe 58	PCIe 60	SATA 58	SATA 58
	PCIe 59	PCIe 61	SATA 59	SATA 59
	PCIe 60	PCIe 62	SATA 60	SATA 60
	PCIe 61	PCIe 63	SATA 61	SATA 61
	PCIe 62	PCIe 64	SATA 62	SATA 62
	PCIe 63	PCIe 65	SATA 63	SATA 63
	PCIe 64	PCIe 66	SATA 64	SATA 64
	PCIe 65	PCIe 67	SATA 65	SATA 65
	PCIe 66	PCIe 68	SATA 66	SATA 66
	PCIe 67	PCIe 69	SATA 67	SATA 67
	PCIe 68	PCIe 70	SATA 68	SATA 68
	PCIe 69	PCIe 71	SATA 69	SATA 69
	PCIe 70	PCIe 72	SATA 70	SATA 70
	PCIe 71	PCIe 73	SATA 71	SATA 71
	PCIe 72	PCIe 74	SATA 72	SATA 72
	PCIe 73	PCIe 75	SATA 73	SATA 73
	PCIe 74	PCIe 76	SATA 74	SATA 74
	PCIe 75	PCIe 77	SATA 75	SATA 75
	PCIe 76	PCIe 78	SATA 76	SATA 76
	PCIe 77	PCIe 79	SATA 77	SATA 77
	PCIe 78	PCIe 80	SATA 78	SATA 78
	PCIe 79	PCIe 81	SATA 79	SATA 79
	PCIe 80	PCIe 82	SATA 80	SATA 80
	PCIe 81	PCIe 83	SATA 81	SATA 81
	PCIe 82	PCIe 84	SATA 82	SATA 82
	PCIe 83	PCIe 85	SATA 83	SATA 83
	PCIe 84	PCIe 86	SATA 84	SATA 84
	PCIe 85	PCIe 87	SATA 85	SATA 85
	PCIe 86	PCIe 88	SATA 86	SATA 86
	PCIe 87	PCIe 89	SATA 87	SATA 87
	PCIe 88	PCIe 90	SATA 88	SATA 88
	PCIe 89	PCIe 91	SATA 89	SATA 89
	PCIe 90	PCIe 92	SATA 90	SATA 90
	PCIe 91	PCIe 93	SATA 91	SATA 91
	PCIe 92	PCIe 94	SATA 92	SATA 92
	PCIe 93	PCIe 95	SATA 93	SATA 93
	PCIe 94	PCIe 96	SATA 94	SATA 94
	PCIe 95	PCIe 97	SATA 95	SATA 95
	PCIe 96	PCIe 98	SATA 96	SATA 96
	PCIe 97	PCIe 99	SATA 97	SATA 97
	PCIe 98	PCIe 100	SATA 98	SATA 98
	PCIe 99	PCIe 101	SATA 99	SATA 99
	PCIe 100	PCIe 102	SATA 100	SATA 100
	PCIe 101	PCIe 103	SATA 101	SATA 101
	PCIe 102	PCIe 104	SATA 102	SATA 102
	PCIe 103	PCIe 105	SATA 103	SATA 103
	PCIe 104	PCIe 106	SATA 104	SATA 104
	PCIe 105	PCIe 107	SATA 105	SATA 105
	PCIe 106	PCIe 108	SATA 106	SATA 106
	PCIe 107	PCIe 109	SATA 107	SATA 107
	PCIe 108	PCIe 110	SATA 108	SATA 108
	PCIe 109	PCIe 111	SATA 109	SATA 109
	PCIe 110	PCIe 112	SATA 110	SATA 110
	PCIe 111	PCIe 113	SATA 111	SATA 111
	PCIe 112	PCIe 114	SATA 112	SATA 112
	PCIe 113	PCIe 115	SATA 113	SATA 113
	PCIe 114	PCIe 116	SATA 114	SATA 114
	PCIe 115	PCIe 117	SATA 115	SATA 115
	PCIe 116	PCIe 118	SATA 116	SATA 116
	PCIe 117	PCIe 119	SATA 117	SATA 117
	PCIe 118	PCIe 120	SATA 118	SATA 118
	PCIe 119	PCIe 121	SATA 119	SATA 119
	PCIe 120	PCIe 122	SATA 120	SATA 120
	PCIe 121	PCIe 123	SATA 121	SATA 121
	PCIe 122	PCIe 124	SATA 122	SATA 122
	PCIe 123	PCIe 125	SATA 123	SATA 123
	PCIe 124	PCIe 126	SATA 124	SATA 124
	PCIe 125	PCIe 127	SATA 125	SATA 125
	PCIe 126	PCIe 128	SATA 126	SATA 126
	PCIe 127	PCIe 129	SATA 127	SATA 127
	PCIe 128	PCIe 130	SATA 128	SATA 128
	PCIe 129	PCIe 131	SATA 129	SATA 129
	PCIe 130	PCIe 132	SATA 130	SATA 130
	PCIe 131	PCIe 133	SATA 131	SATA 131
	PCIe 132	PCIe 134	SATA 132	SATA 132
	PCIe 133	PCIe 135	SATA 133	SATA 133
	PCIe 134	PCIe 136	SATA 134	SATA 134
	PCIe 135	PCIe 137	SATA 135	SATA 135
	PCIe 136	PCIe 138	SATA 136	SATA 136
	PCIe 137	PCIe 139	SATA 137	SATA 137
	PCIe 138	PCIe 140	SATA 138	SATA 138
	PCIe 139	PCIe 141	SATA 139	SATA 139
	PCIe 140	PCIe 142	SATA 140	SATA 140
	PCIe 141	PCIe 143	SATA 141	SATA 141
	PCIe 142	PCIe 144	SATA 142	SATA 142
	PCIe 143	PCIe 145	SATA 143	SATA 143
	PCIe 144	PCIe 146	SATA 144	SATA 144
	PCIe 145	PCIe 147	SATA 145	SATA 145
	PCIe 146	PCIe 148	SATA 146	SATA 146
	PCIe 147	PCIe 149	SATA 147	SATA 147
	PCIe 148	PCIe 150	SATA 148	SATA 148
	PCIe 149	PCIe 151	SATA 149	SATA 149
	PCIe 150	PCIe 152	SATA 150	SATA 150
	PCIe 151	PCIe 153	SATA 151	SATA 151
	PCIe 152	PCIe 154	SATA 152	SATA 152
	PCIe 153	PCIe 155	SATA 153	SATA 153
	PCIe 154	PCIe 156	SATA 154	SATA 154
	PCIe 155	PCIe 157	SATA 155	SATA 155
	PCIe 156	PCIe 158	SATA 156	SATA 156
	PCIe 157	PCIe 159	SATA 157	SATA 157
	PCIe 158	PCIe 160	SATA 158	SATA 158
	PCIe 159	PCIe 161	SATA 159	SATA 159
	PCIe 160	PCIe 162	SATA 160	SATA 160
	PCIe 161	PCIe 163	SATA 161	SATA 161
	PCIe 162	PCIe 164	SATA 162	SATA 162
	PCIe 163	PCIe 165	SATA 163	SATA 163
	PCIe 164	PCIe 166	SATA 164	SATA 164
	PCIe 165	PCIe 167	SATA 165	SATA 165
	PCIe 166	PCIe 168	SATA 166	SATA 166
	PCIe 167	PCIe 169	SATA 167	SATA 167
	PCIe 168	PCIe 170	SATA 168	SATA 168
	PCIe 169	PCIe 171	SATA 169	SATA 169
	PCIe 170	PCIe 172	SATA 170	SATA 170
	PCIe 171	PCIe 173	SATA 171	SATA 171
	PCIe 172	PCIe 174	SATA 172	SATA 172
	PCIe 173	PCIe 175	SATA 173	SATA 173
	PCIe 174	PCIe 176	SATA 174	SATA 174
	PCIe 175	PCIe 177	SATA 175	SATA 175
	PCIe 176	PCIe 178	SATA 176	SATA 176
	PCIe 177	PCIe 179	SATA 177	SATA 177
	PCIe 178	PCIe 180	SATA 178	SATA 178
	PCIe 179	PCIe 181	SATA 179	SATA 179
	PCIe 180	PCIe 182	SATA 180	SATA 180
	PCIe 181	PCIe 183	SATA 181	SATA 181
	PCIe 182	PCIe 184	SATA 182	SATA 182
	PCIe 183	PCIe 185	SATA 183	SATA 183
	PCIe 184	PCIe 186	SATA 184	SATA 184
	PCIe 185	PCIe 187	SATA 185	SATA 185
	PCIe 186	PCIe 188	SATA 186	SATA 186
	PCIe 187	PCIe 189	SATA 187	SATA 187
	PCIe 188	PCIe 190	SATA 188	SATA 188
	PCIe 189	PCIe 191	SATA 189	SATA 189
	PCIe 190	PCIe 192	SATA 190	SATA 190
	PCIe 191	PCIe 193	SATA 191	SATA 191
	PCIe 192	PCIe 194	SATA 192	SATA 192
	PCIe 193	PCIe 195	SATA 193	SATA 193
	PCIe 194	PCIe 196	SATA 194	SATA 194
	PCIe 195	PCIe 197	SATA 195	SATA 195
	PCIe 196	PCIe 198	SATA 196	SATA 196
	PCIe 197	PCIe 199	SATA 197	SATA 197
	PCIe 198	PCIe 200	SATA 198	SATA 198
	PCIe 199	PCIe 201	SATA 199	SATA 199
	PCIe 200	PCIe 202	SATA 200	SATA 200
	PCIe 201	PCIe 203	SATA 201	SATA 201
	PCIe 202	PCIe 204	SATA 202	SATA 202
	PCIe 203	PCIe 205	SATA 203	SATA 203
	PCIe 204	PCIe 206	SATA 204	SATA 204
	PCIe 205	PCIe 207	SATA 205	SATA 205
	PCIe 206	PCIe 208	SATA 206	SATA 206
	PCIe 207	PCIe 209	SATA 207	SATA 207
	PCIe 208	PCIe 210	SATA 208	SATA 208
	PCIe 209	PCIe 211	SATA 209	SATA 209
	PCIe 210	PCIe 212	SATA 210	SATA 210
	PCIe 211	PCIe 213	SATA 211	SATA 211
	PCIe 212	PCIe 214	SATA 212	SATA 212
	PCIe 213	PCIe 215	SATA 213	SATA 213
	PCIe 214	PCIe 216	SATA 214	SATA 214
	PCIe 215	PCIe 217	SATA 215	SATA 215
	PCIe 216	PCIe 218	SATA 216	SATA 216
	PCIe 217	PCIe 219	SATA 217	SATA 217
	PCIe 218	PCIe 220	SATA 218	SATA 218
	PCIe 219	PCIe 221	SATA 219	SATA 219
	PCIe 220	PCIe 222	SATA 220	SATA 220
	PCIe 221	PCIe 223	SATA 221	SATA 221
	PCIe 222	PCIe 224	SATA 222	SATA 222
	PCIe 223	PCIe 225	SATA 223	SATA 223
	PCIe 224	PCIe 226	SATA 224	SATA 224
	PCIe 225	PCIe 227	SATA 225	SATA 225
	PCIe 226	PCIe 228	SATA 226	SATA 226
	PCIe 227	PCIe 229	SATA 227	SATA

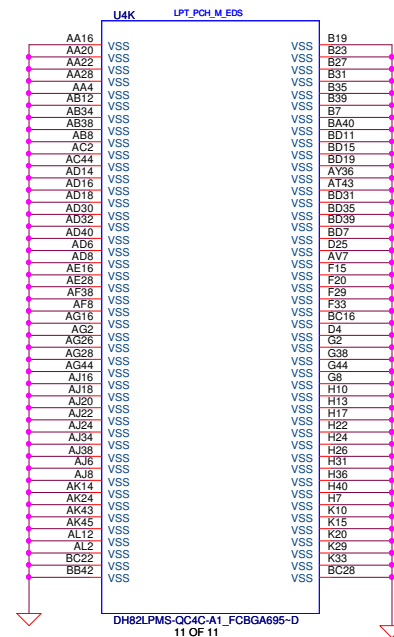
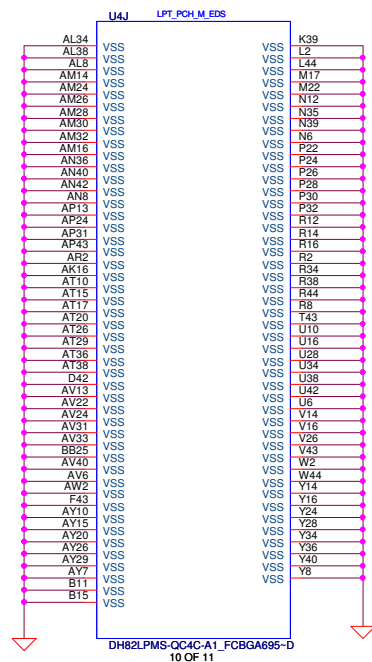


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



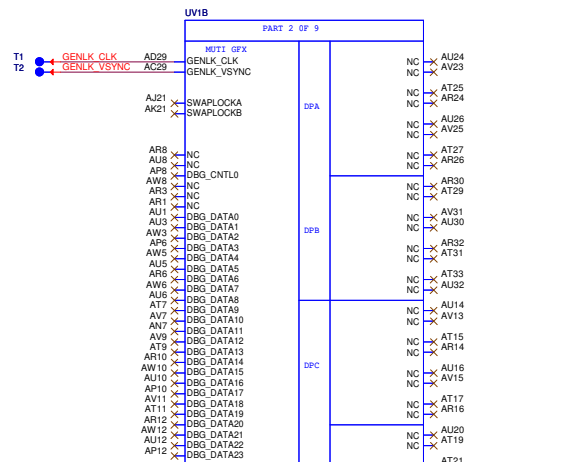
PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc. PCH (8/9) PWR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED TO REPRODUCE OR IN ANY MANNER DISCLOSE TO ANY THIRD PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document Number	0.1
				Custom	LA-9641P
				Date:	Thursday, October 11, 2012
				Sheet	21 of 60

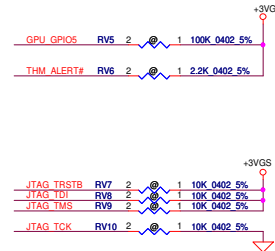


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	PCH (9/9) VSS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT OF DEFENSE OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9641P
				Date	Thursday, October 11, 2012
				Sheet	22 of 60
				Rev	0.1





## STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

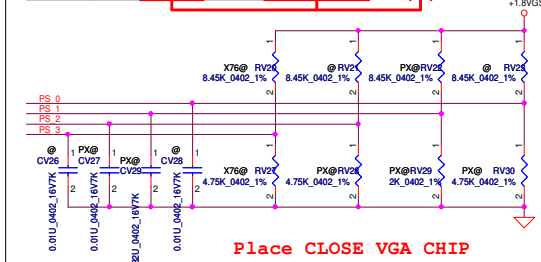
RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 10K RESISTOR  
 X= DESIGN DEPENDANT  
 NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRs_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100-512Kbit M2SP05A (ST) 101-1Mbit M2SP10A (ST) 101-2Mbit M2SP20 (ST) 101-4Mbit M2SP40 (ST) 101-8Mbit M2SP80 (ST) 100-512Kbit Pm2SLV010 (Chingss) 101-1Mbit Pm2SLV010 (Chingss)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1]	NA	00- No audio function 01- Audio for DP only 10- Audio for DP and HDMI if dongle is detected 11- Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whisper/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111= 0 usable endpoints 110= 1 usable endpoints 101= 2 usable endpoints 100= 3 usable endpoints 011= 4 usable endpoints 010= 5 usable endpoints 001= 6 usable endpoints 000= all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

## MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_1[5:1]	0 1	0 0 1	82 nF	8.45K	2K
PS_2[5:1]	1 0	0 0 0	10 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 4



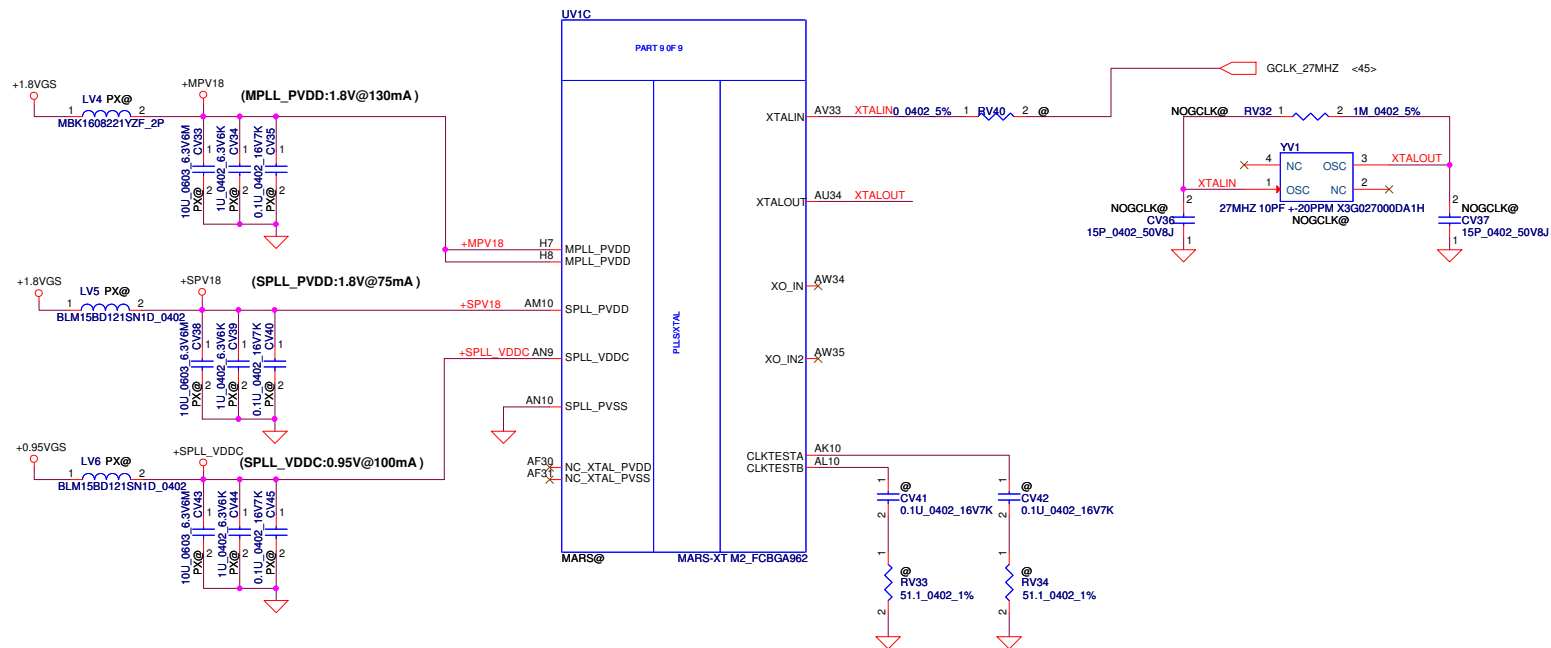
Place CLOSE VGA CHIP



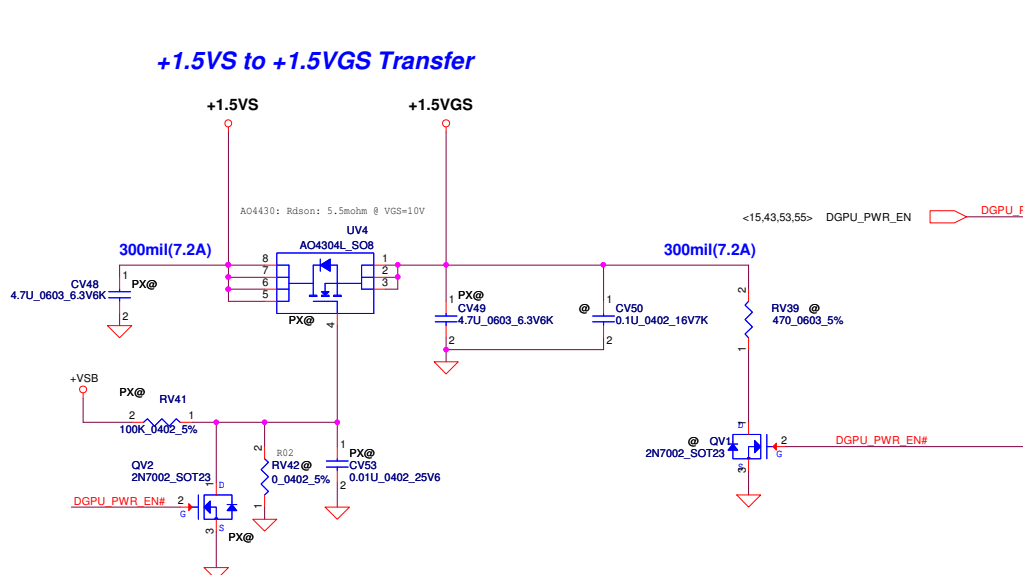
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

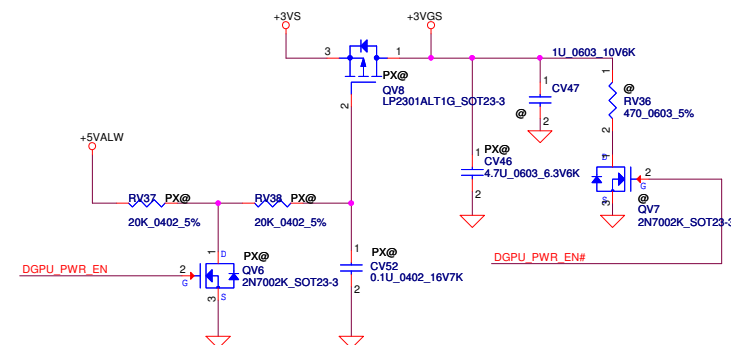


### +1.5VS to +1.5VGS Transfer



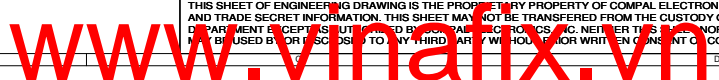
### <+3VS TO +3VGS>

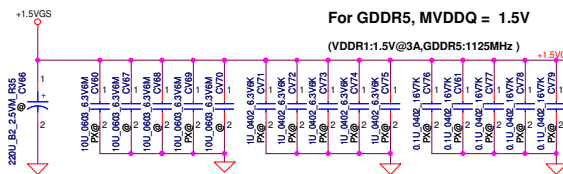
Need OPEN



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/07/03				Deciphered Date			
								2013/07/03			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Title				AT1 MarsXTX M2 BACO POWER			
				Document Number				LA8642P M/B			
				Rev				0.1			
				Date				Thursday, October 11, 2012			
				Sheet				25 of 60			

www.vitalix.vn



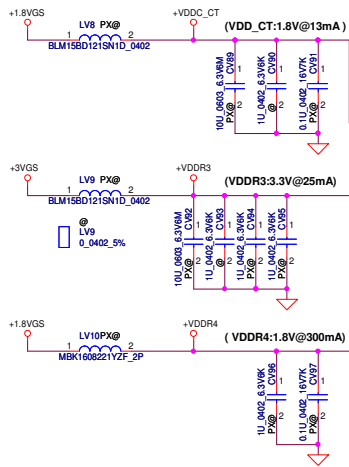


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

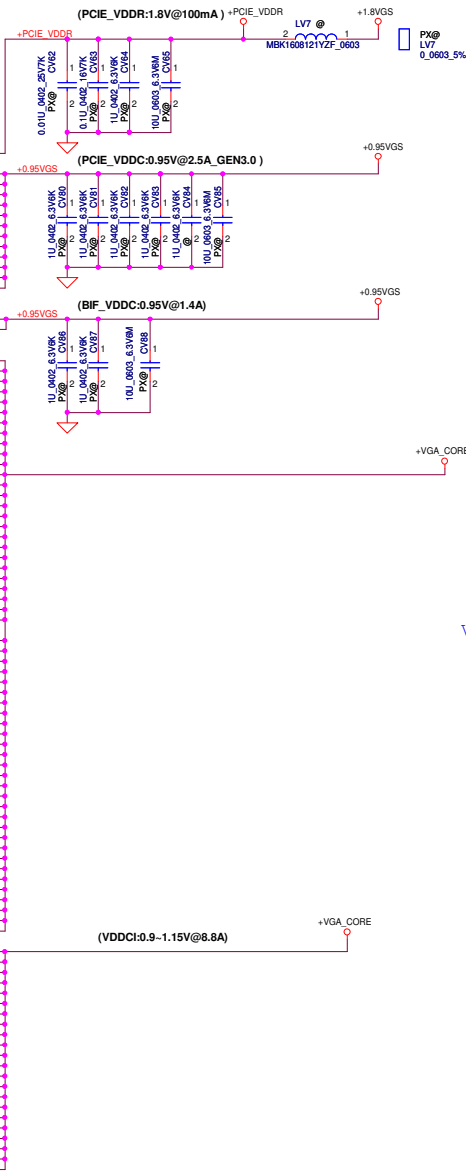
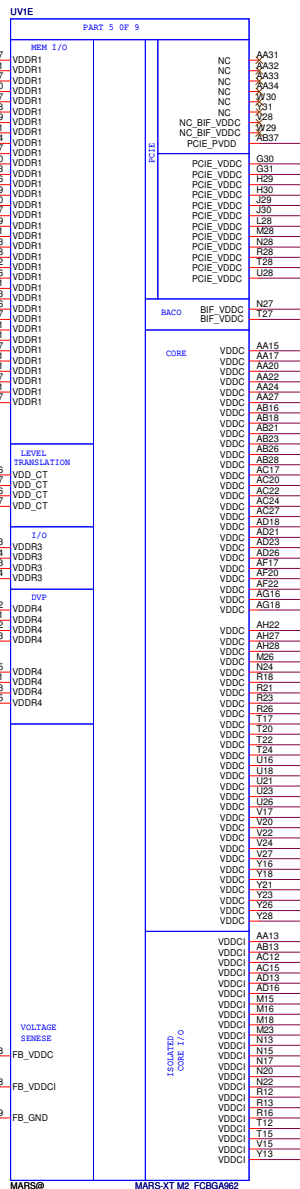
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



Route as differential pair



PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA\_CORE Cap in power side sheet



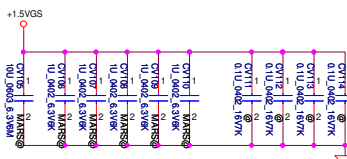
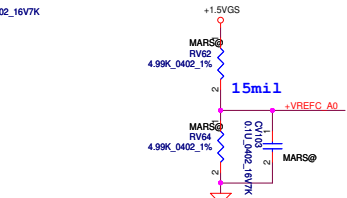
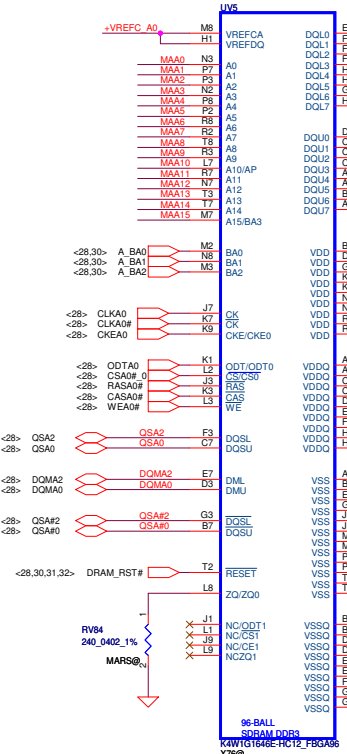
<28. MDA[0..31] MDA[0..31]

<28.30> MAA[15..0] MAA[15..0]

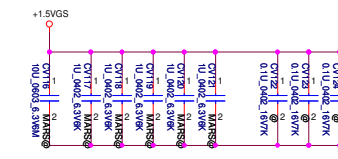
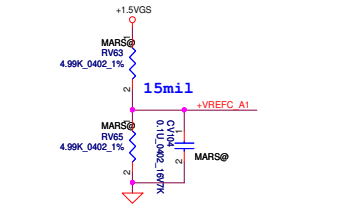
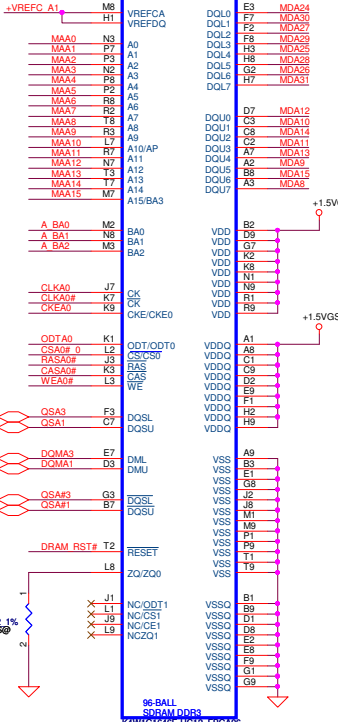
CLKA0\_1 MARS@ 40.2\_0402\_1% RV60

CLKA0#1 MARS@ 40.2\_0402\_1% RV61

CV195 0.01U\_0402\_16V7K MARS@



+1.5VGS



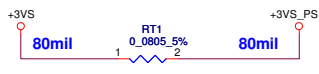
Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2010/08/25	Deciphered Date
2012/08/25		ATI Whistler M2 VRAM A
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. NO PART OF THIS SHEET IS TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.		Document Number
QIY2 LA6884P		Rev 1.0
Date: Thursday, October 11, 2012		Sheet 29 of 60



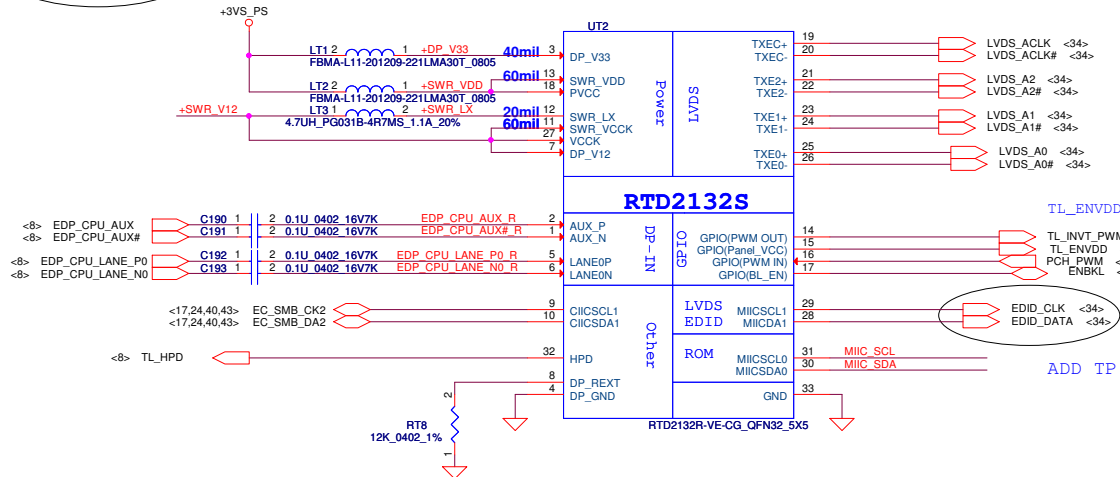
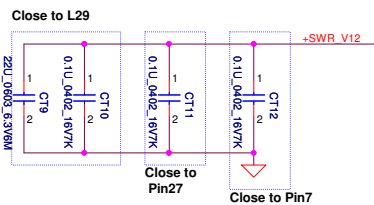
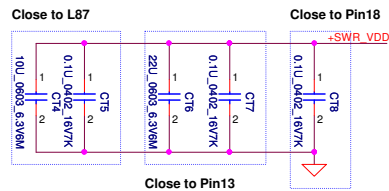
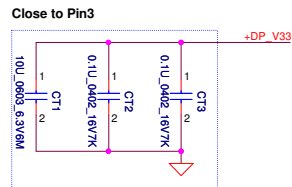
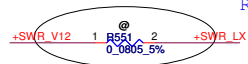






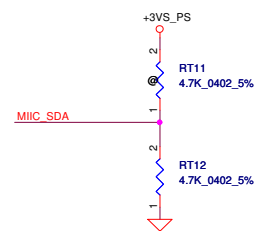
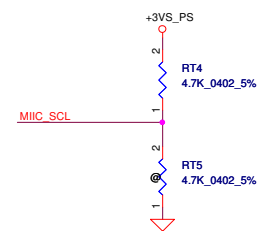
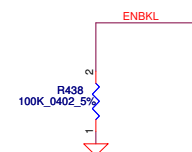
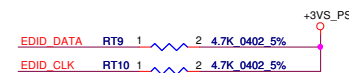


# RTD2132R LDO MODE



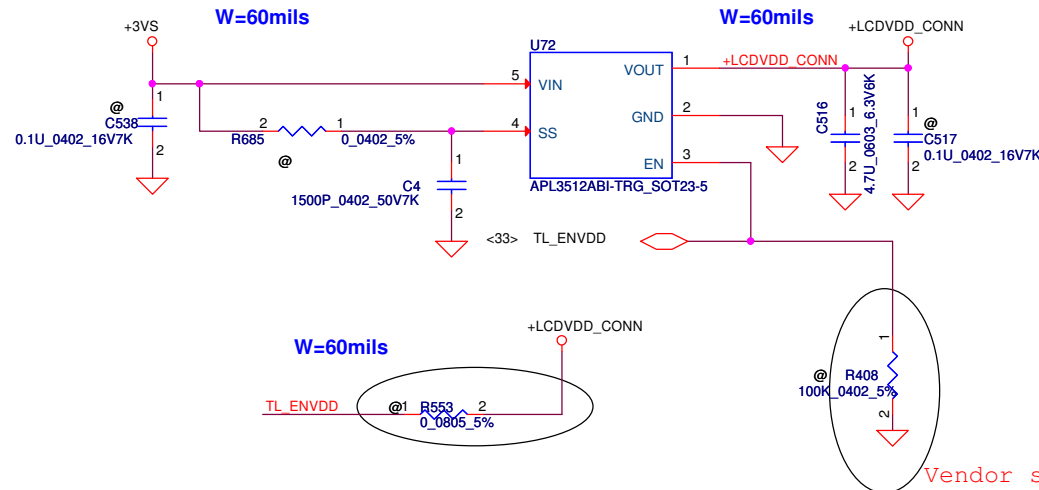
TL\_ENVDD need 60 mil if use for LVDS power on R version

ADD TP on trace or via

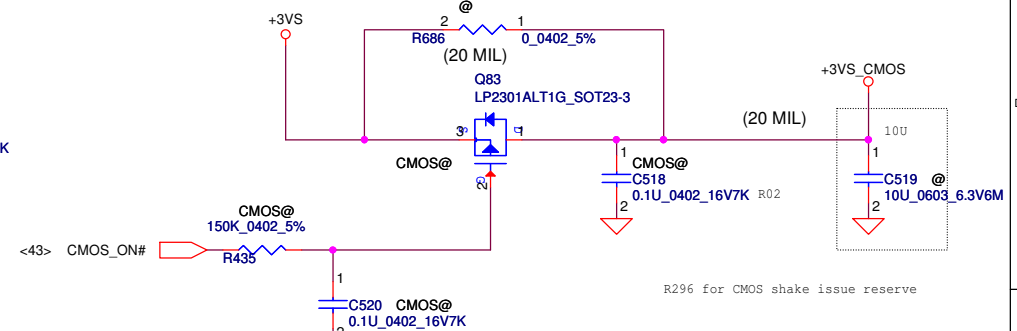


MIIC_SCL \ MIIC_SDA	0	1
	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

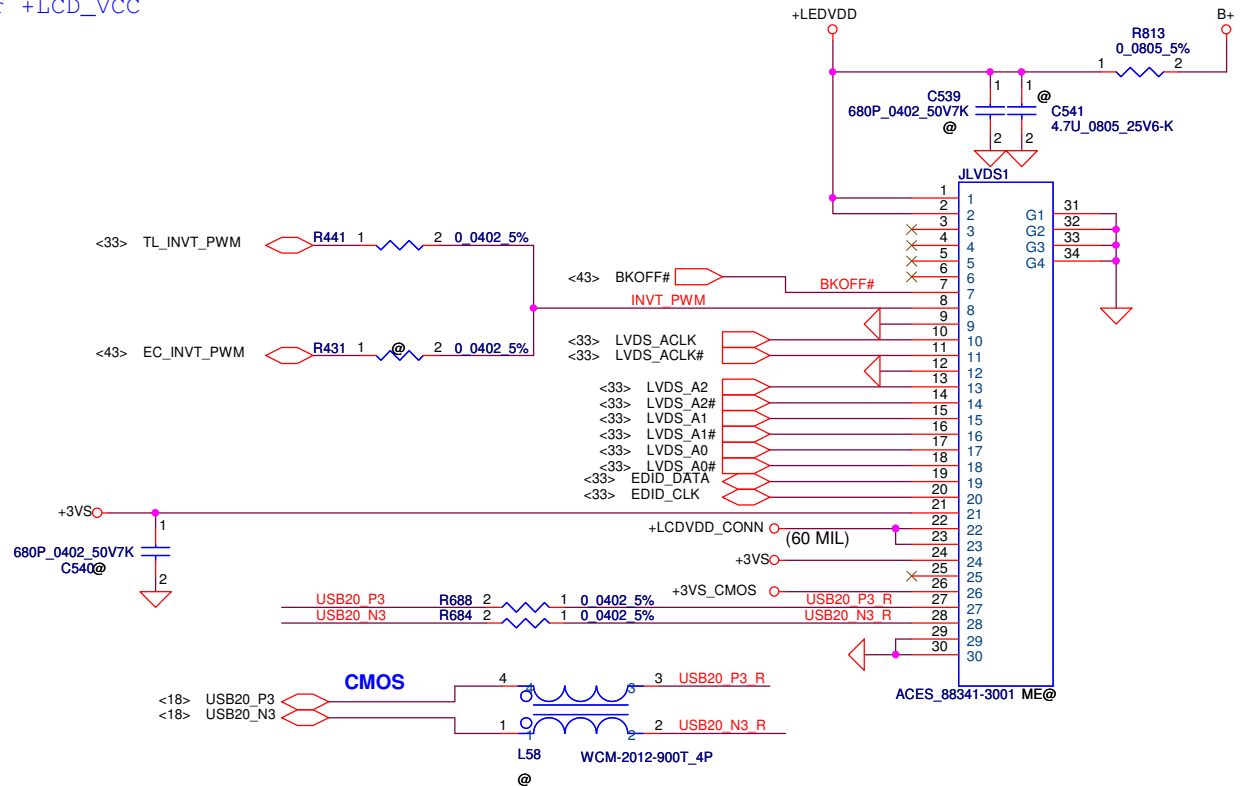
# LCD POWER CIRCUIT



# CMOS Camera

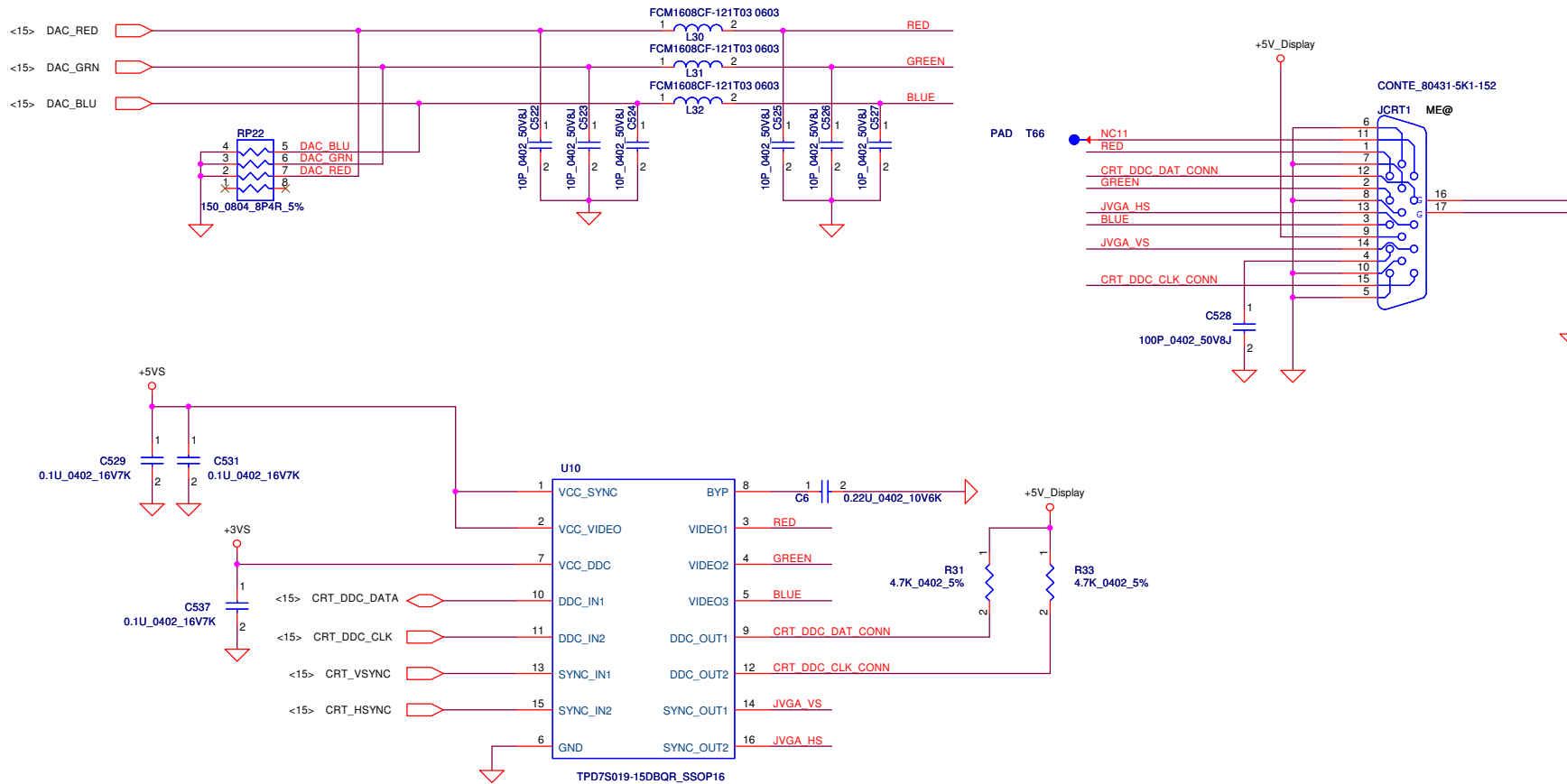


# VGA LCD/PANEL BD. Conn.

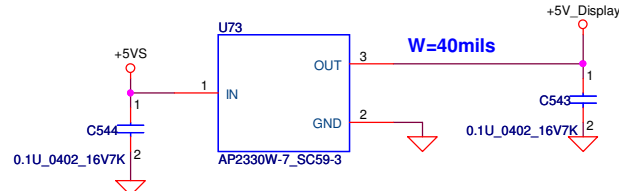
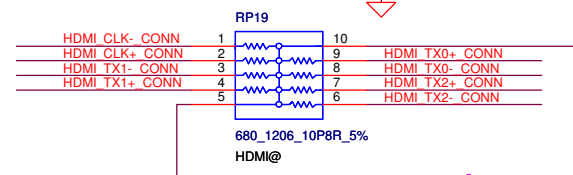
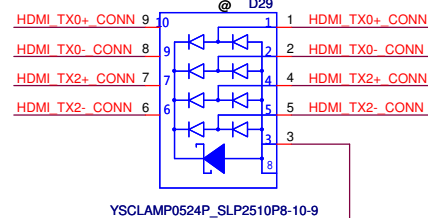


Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO AN THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 2.0
Size	Document Number	LA-9641P		
Date:	Thursday, October 11, 2012	Sheet	34 of 60	

### ***CRT Connector***



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	<b>CRT Connector</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. IN WRITING. THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	<b>LA-9641P</b>	<b>2.0</b>
				Date:	Thursday, October 11, 2012	Sheet 35 of 60

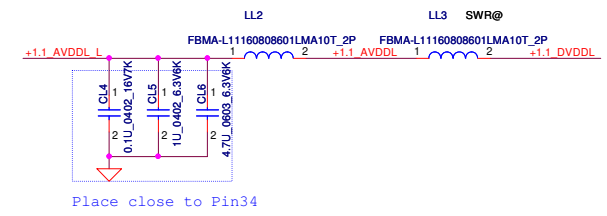
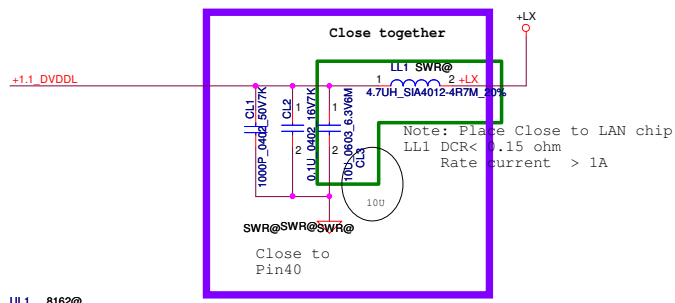
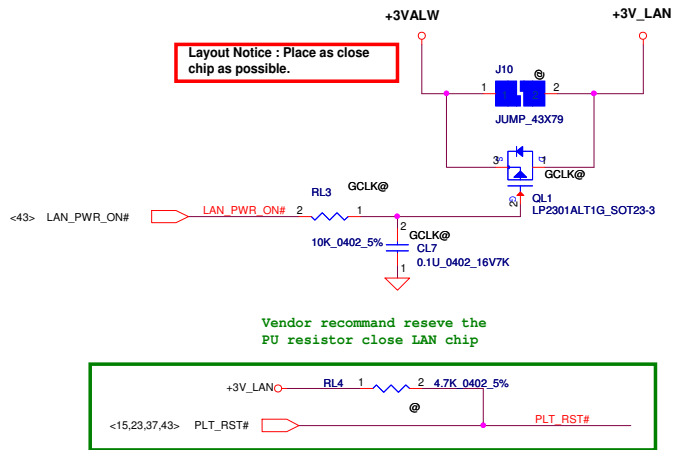


Security Classification	Compal Secret Data			<b>Compal Electronics, Ltd.</b>		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	<b>HDMI CONN</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				5	<b>LA-9641P</b>	2.0
Date: Thursday, October 11, 2012				Sheet	36	of 60

[www.vinafix.vn](http://www.vinafix.vn)

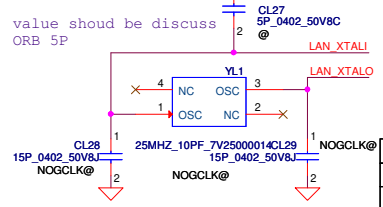
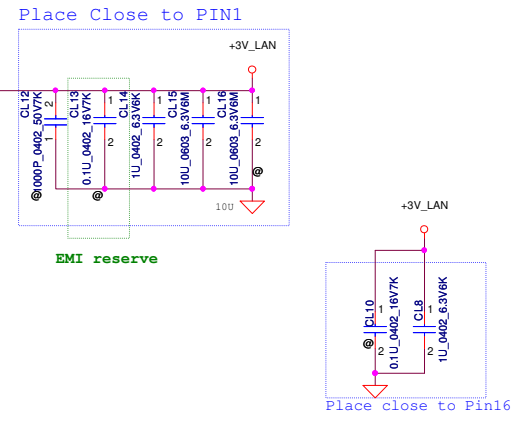
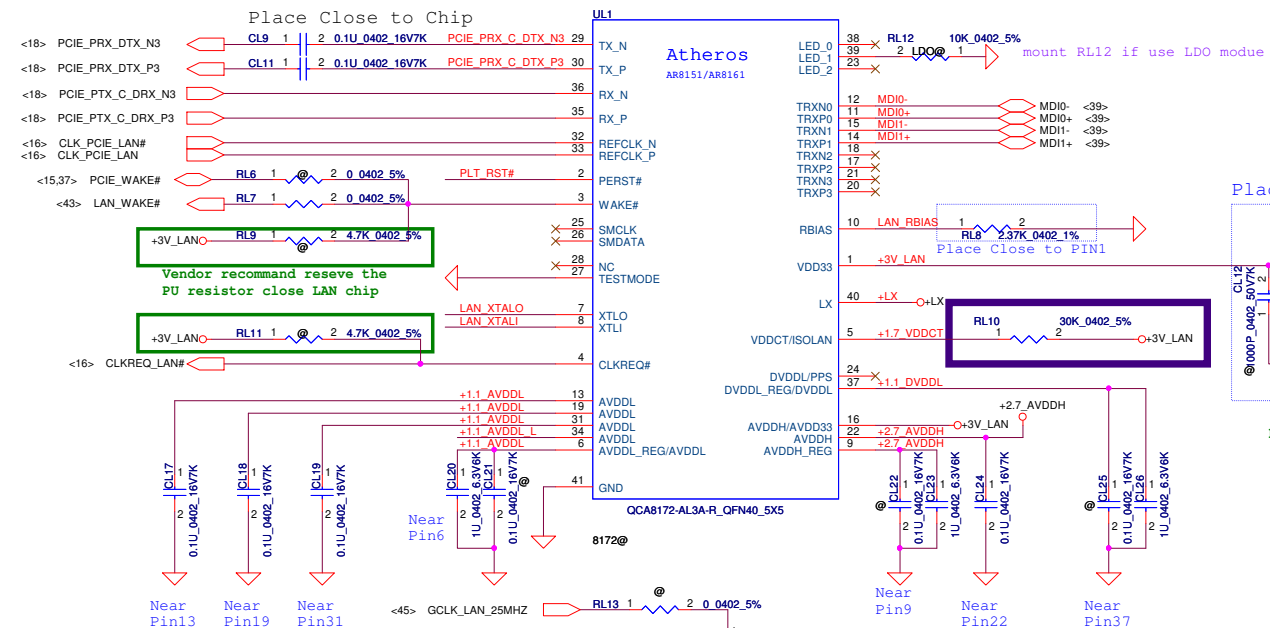


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



UL1 8162@  
AR8162-AL3A-R

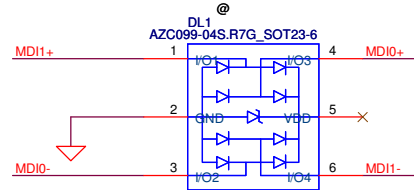
SA000065400 S IC QCA8172-AL3A-R QFN 40P E-LAN CTRL  
SA000052J10 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL



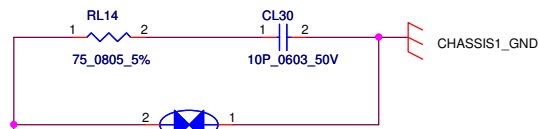
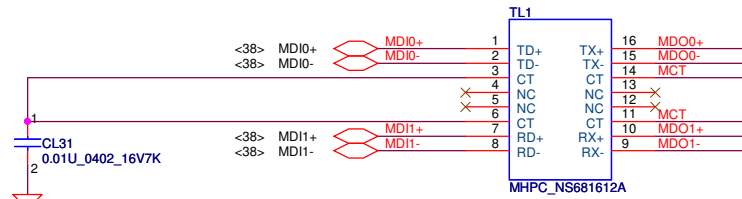
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LAN-AR8162/8172
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7982P
				Date:	Thursday, October 11, 2012
				Sheet	38 of 60

DL1  
1'S PN:SC300001G00  
2'S PN:SC300002E00

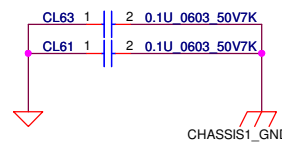
Place Close to TL1



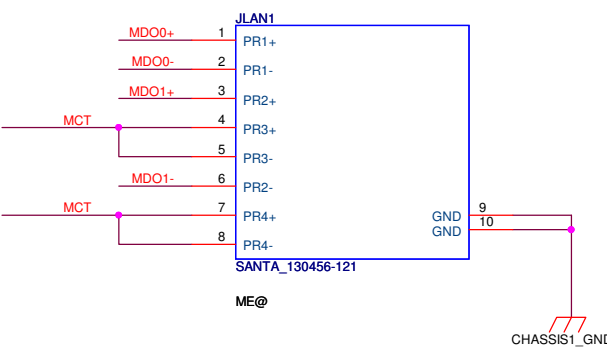
Reserve gas tube for EMI go rural solution



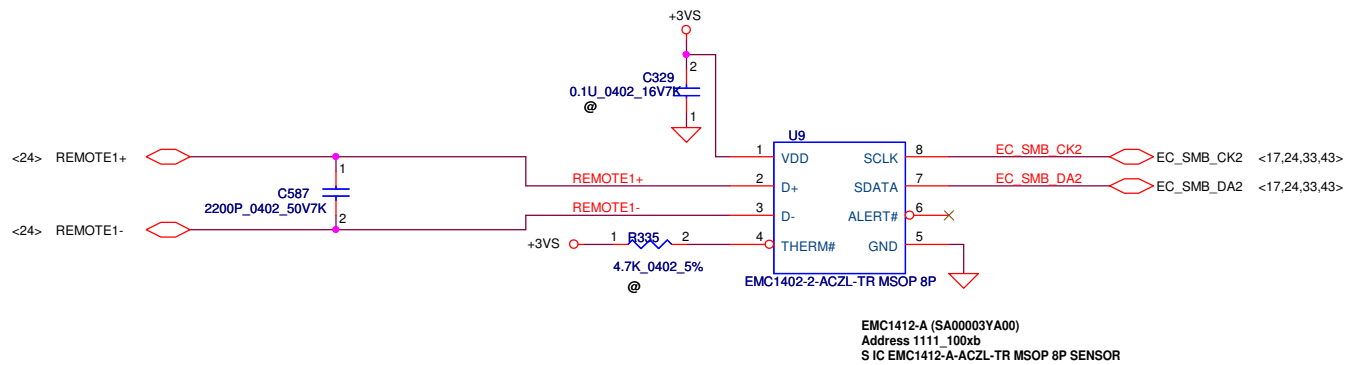
Place Close to TL1



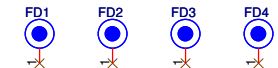
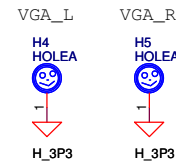
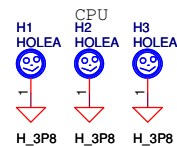
Need check Symbol



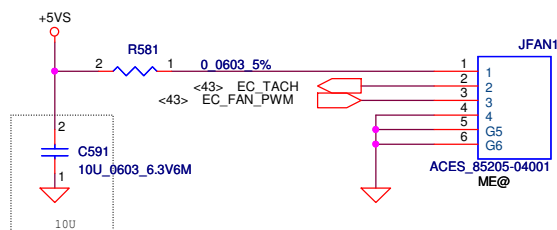
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LAN_Transformer
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7982P
				Date:	Thursday, October 11, 2012
				Sheet	39 of 60



REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



## FAN1 Conn

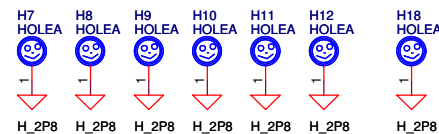


A

B

M/B 橢圓孔

M/B 圓孔



2P8 \* 7 pcd

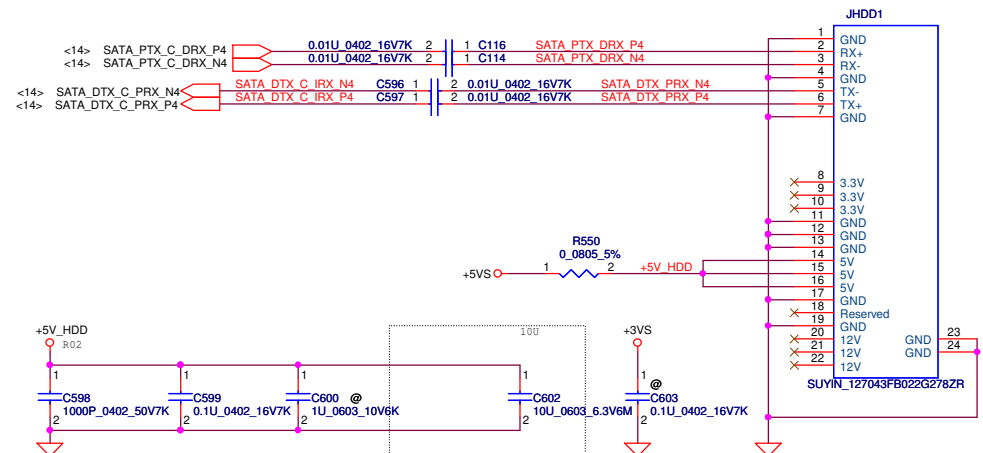
D

E

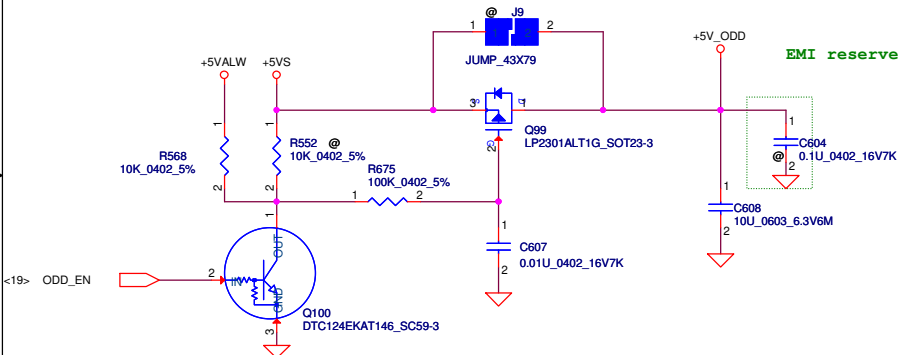
Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Fintek-Thermal IC/FAN/screw
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9641P
				Date: Thursday, October 11, 2012	Sheet 40 of 60



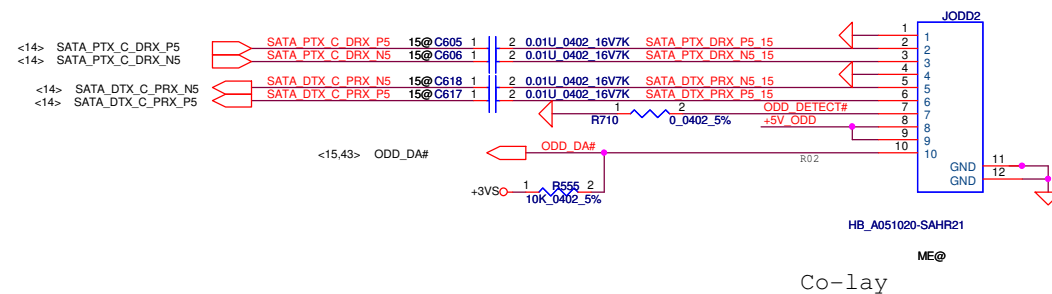
## SATA HDD Conn.



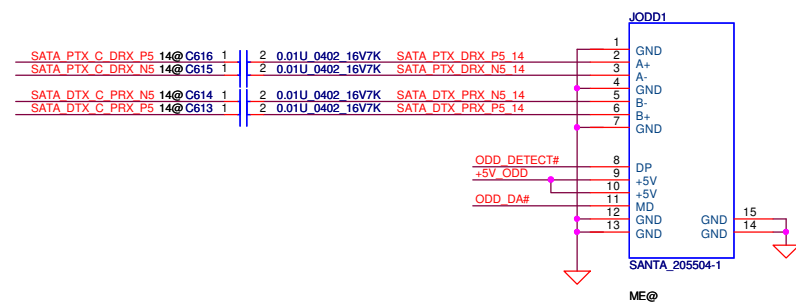
## ODD Power Control



## FOR 15" SATA ODD FFC Conn.



## FOR 14" SATA ODD Conn.



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR FOR ANY OTHER PART WITHIN OR OUTSIDE OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	LA-9641P
				Date	Thursday, October 11, 2012
				Sheet	41 of 60
				Rev	2.0

www.vinalix.vn

CX20751  
High Definition Audio Codec SoC  
With Integrated Class-D Stereo  
Amplifier.  
An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).  
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).

Sense resistors must be  
connected same power  
that is used for VAUX\_3.3

mount RA6 on the Jack Sense circuit  
to configure Port-C for mono MIC.

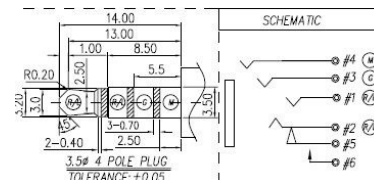
Don't support LINE\_IN function  
RA7 could be @

CA3 vendor suggest  
change to 2.2U

AVDD\_3.3 pins output of  
internal LDO. NOT connect  
to external supply.

Layout Note: Path from +5VS to LPWR\_5.0  
RPWR\_5.0 must be very low  
resistance (<0.01 ohms)

Please bypass caps very close to device.



Check footprint

HGND, HGND 80mils

Pin Ref

1: L

2: R

3: GND/MIC

4: MIC/GND

5: normal open

6: GND

for Universal jack

wide 20MIL

vendor suggest  
change to 100p

SPK R1- CONN

SPK L1- CONN

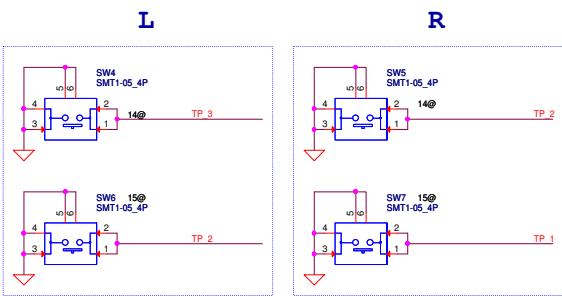
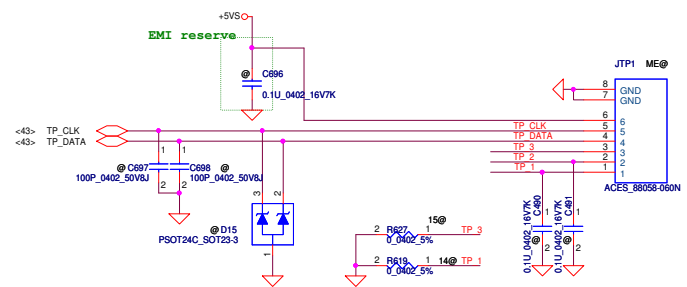
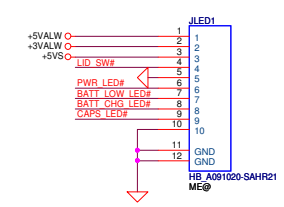
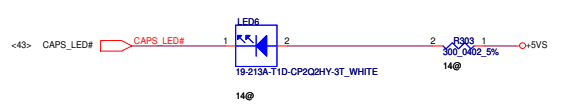
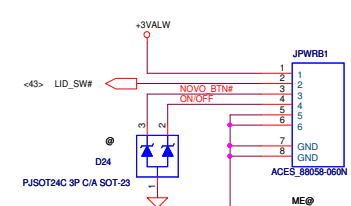
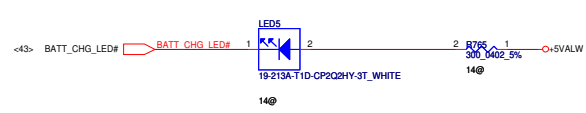
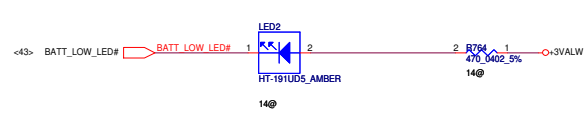
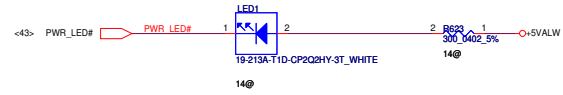
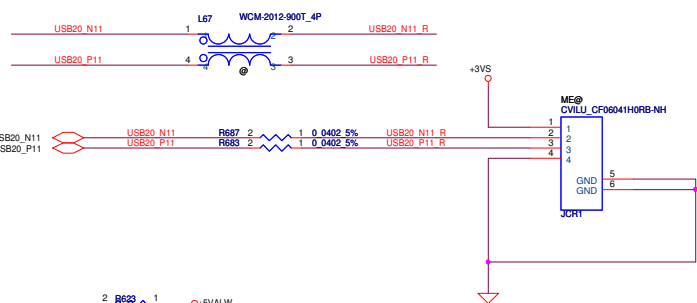
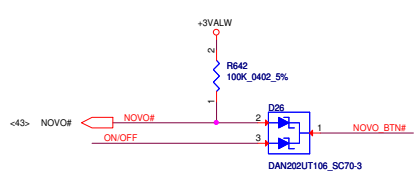
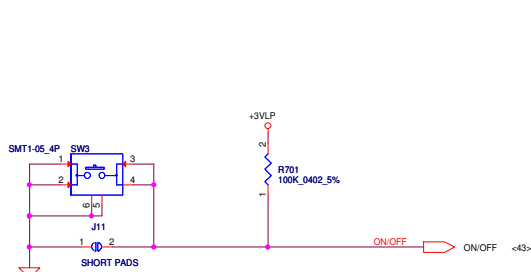
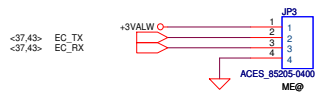
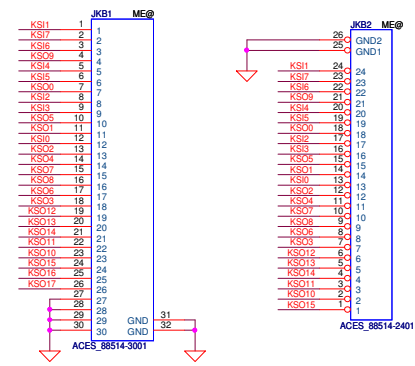
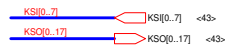
SPK R2- CONN

SPK L2- CONN

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	CX20751 Codec	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custm	LA-7982P
				Date: Thursday, October 11, 2012	Sheet 42 of 60

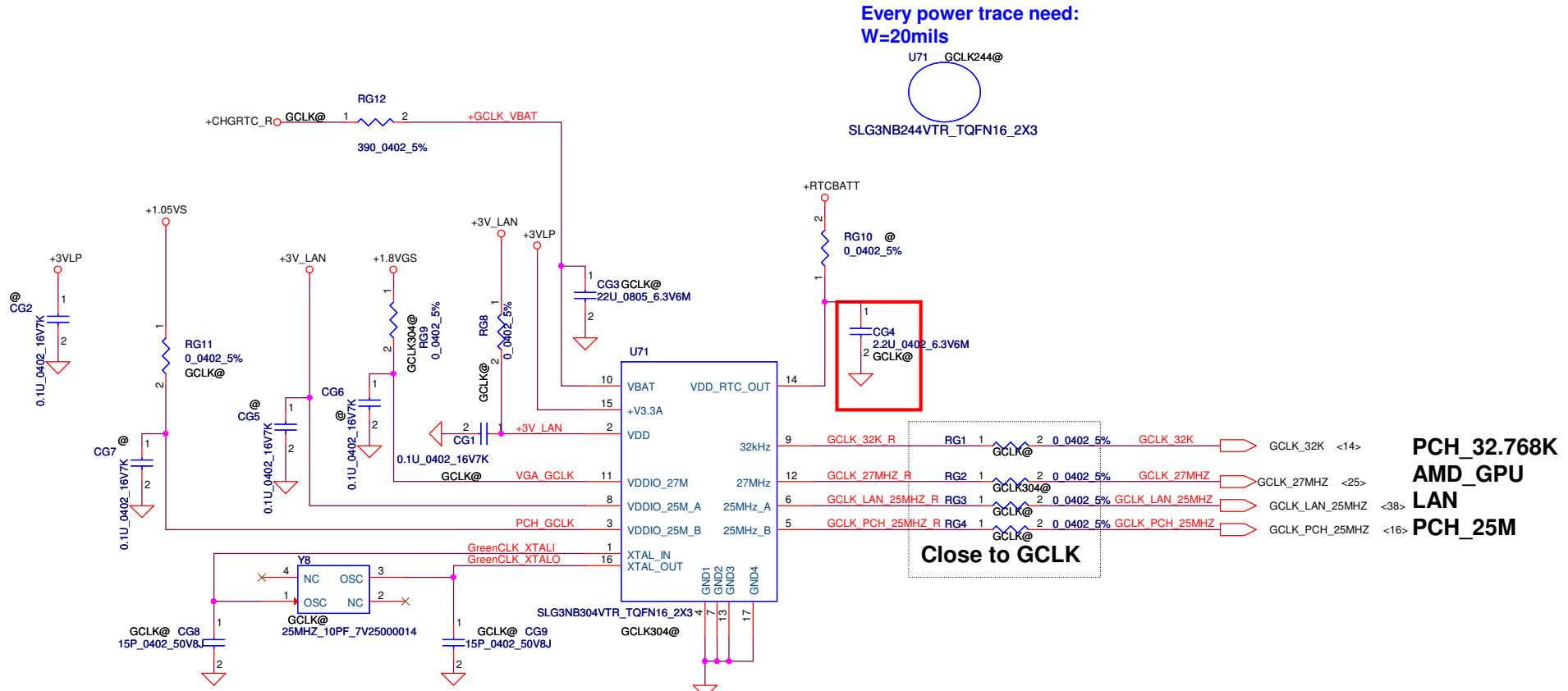
www.vinafix.vn





15"	14"
1 VCC	1 VCC
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 L
5 L	5 R
6 R	6 GND

Green Clock

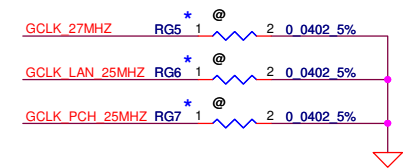


Every power trace need:  
W=20mils



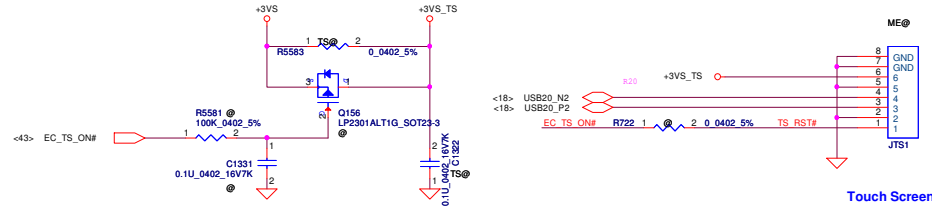
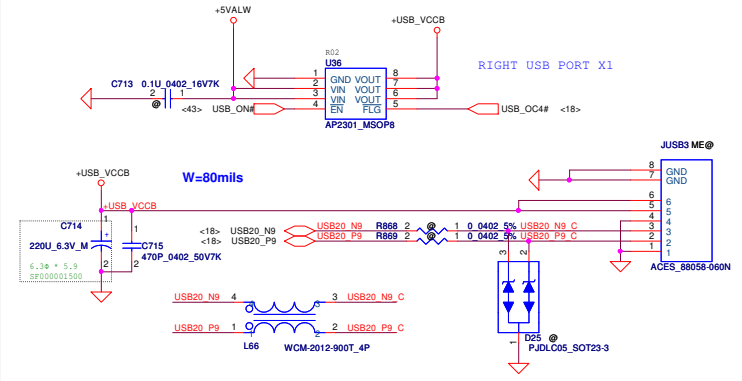
Close to GCLK

Reserved for Swing Level adjustment  
( Close GCLK side )

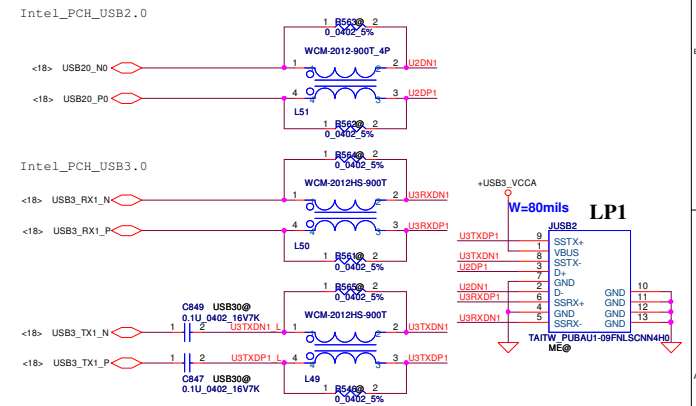
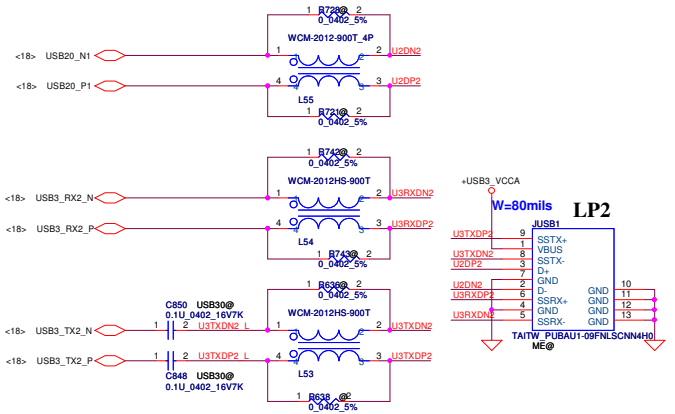
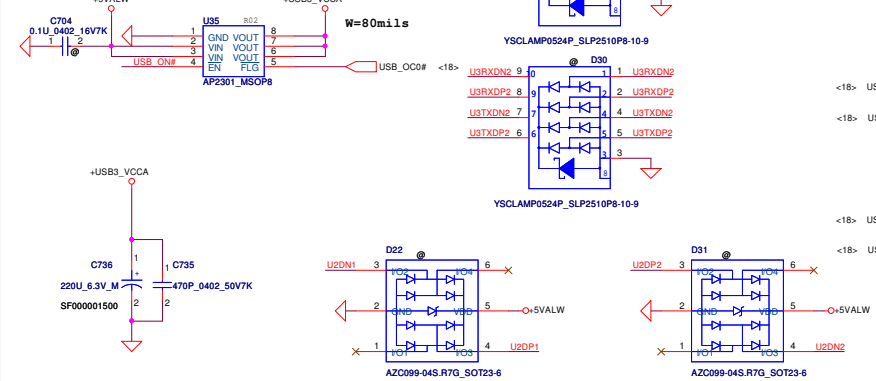


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	USB ext. ports
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9641P
				Date:	Thursday, October 11, 2012
				Sheet	45 of 60

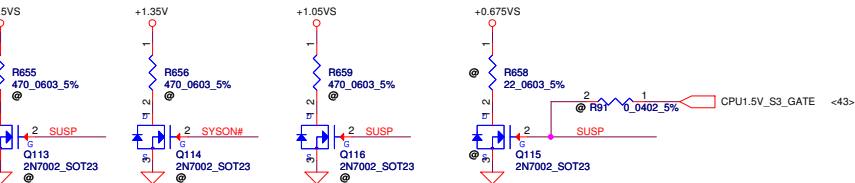
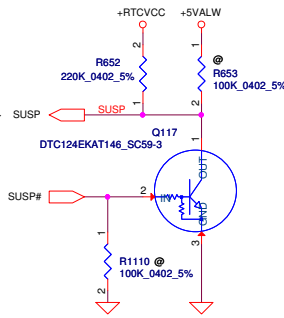
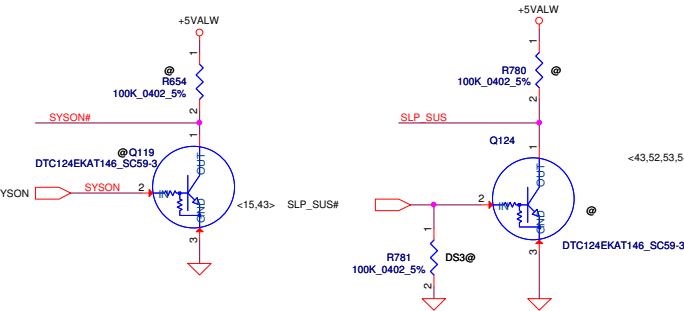
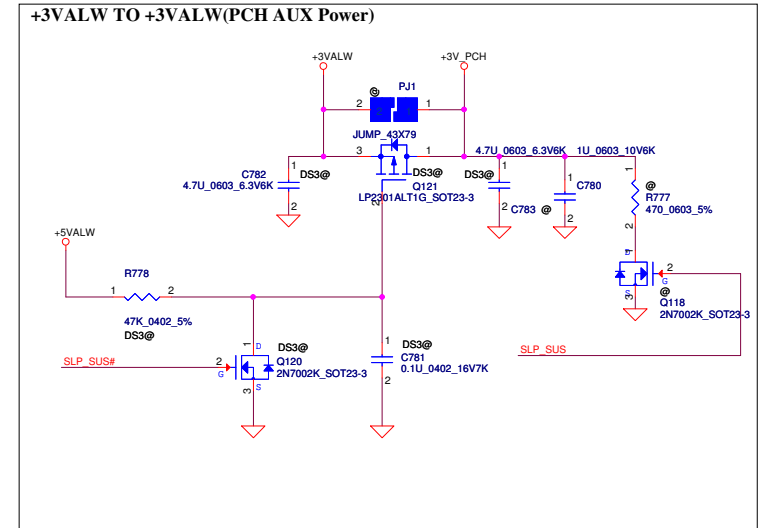
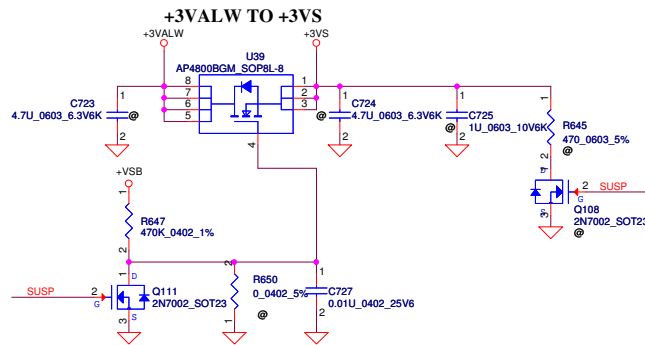
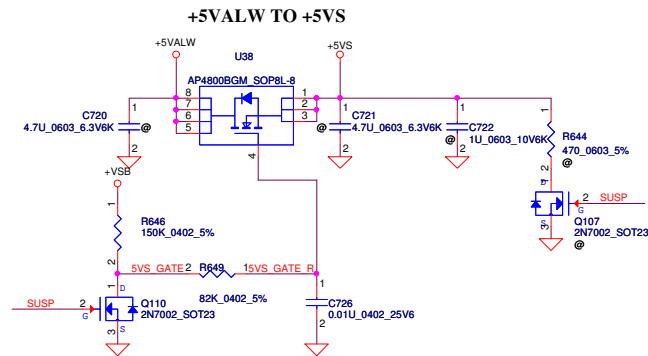
Right Ext.USB Conn.



2A/Active Low

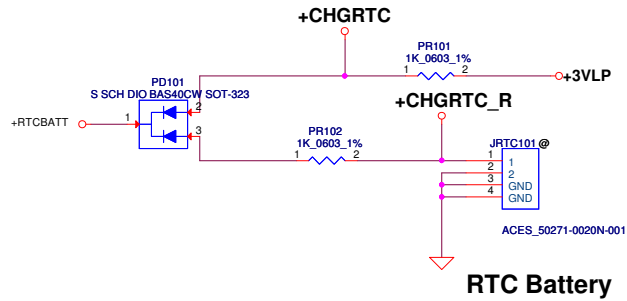
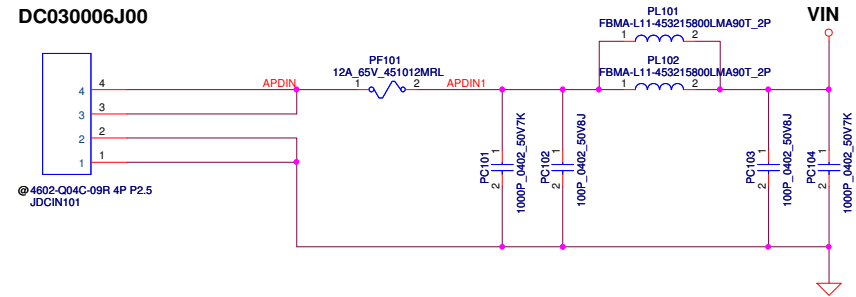


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	USB3.0/Left USB Ports
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 2.0
Size	Document Number	Custom	Date	Thursday, October 11, 2012	Sheet 46 of 60

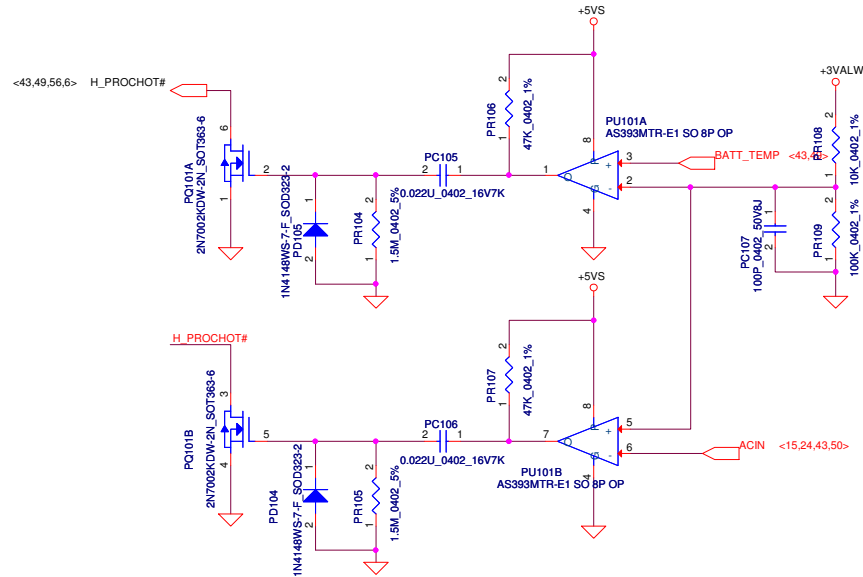


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	DC Interface	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom	2.0
				Date:	Thursday, October 11, 2012
				Sheet	47 of 60

# DC030006J00

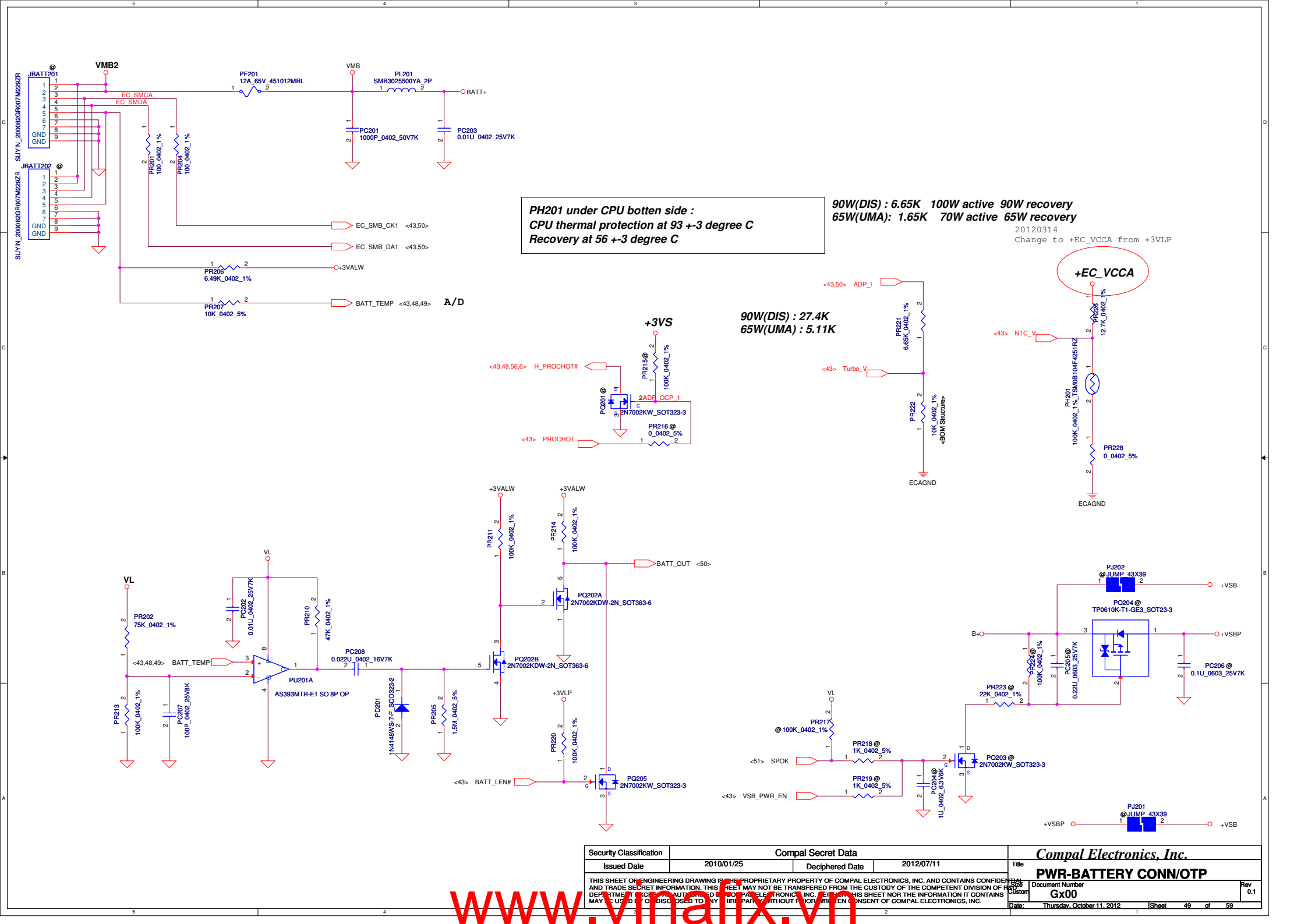


## RTC Battery



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	PWR DCIN / RTC Battery
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIELD DEPARTMENT (FC) OR AUTOMATICALLY DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Gx00
				Date	Thursday, October 11, 2012
				Sheet	48 of 59
				Rev	0.1





PH201 under CPU botten side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery  
65W(UMA): 1.65K 70W active 65W recovery

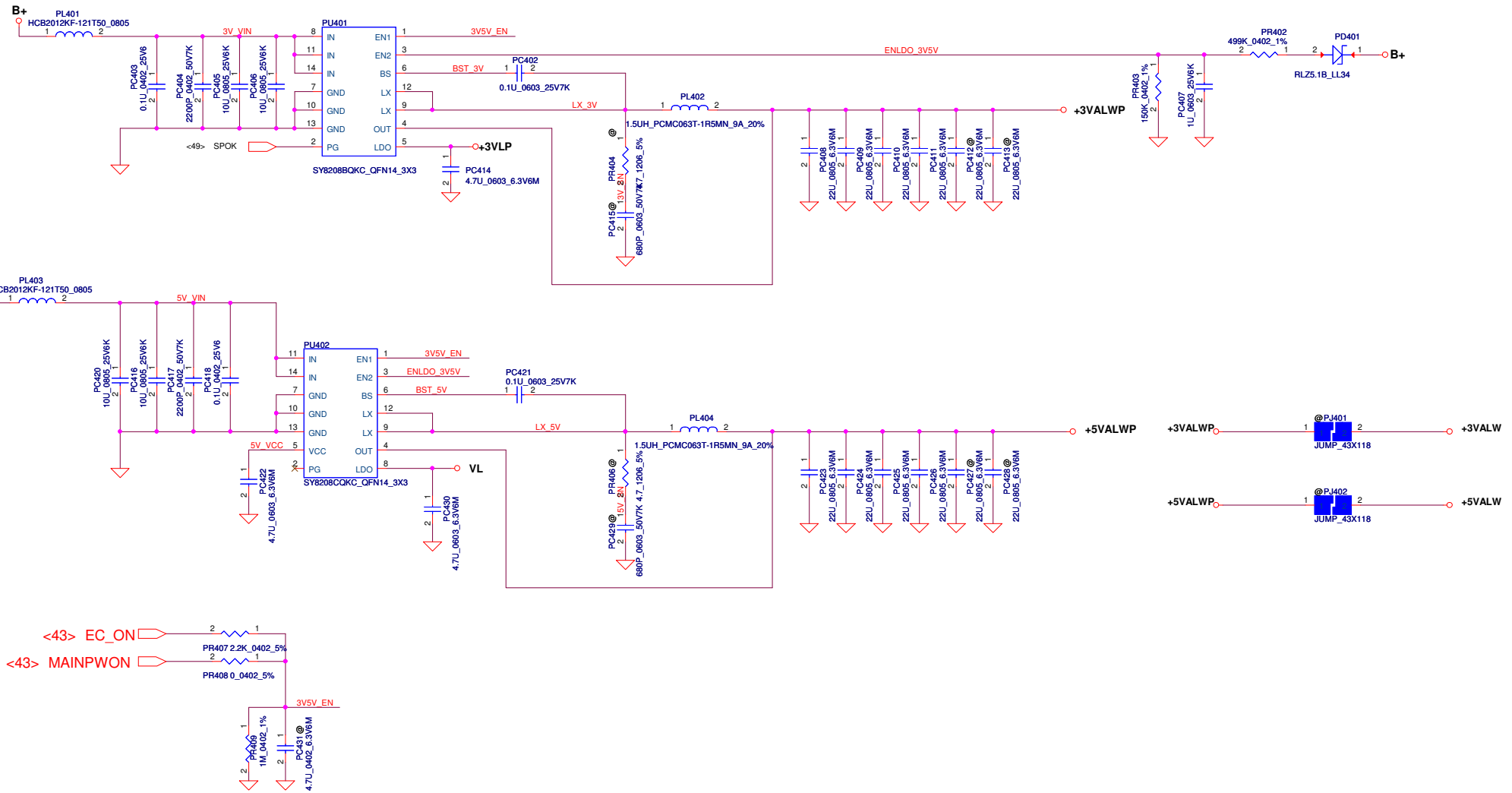
20120314  
Change to +EC\_VCCA from +3VLP

90W(DIS) : 27.4K  
65W(UMA) : 5.11K

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HEADQUARTERS OR ANY SUBSIDIARY OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

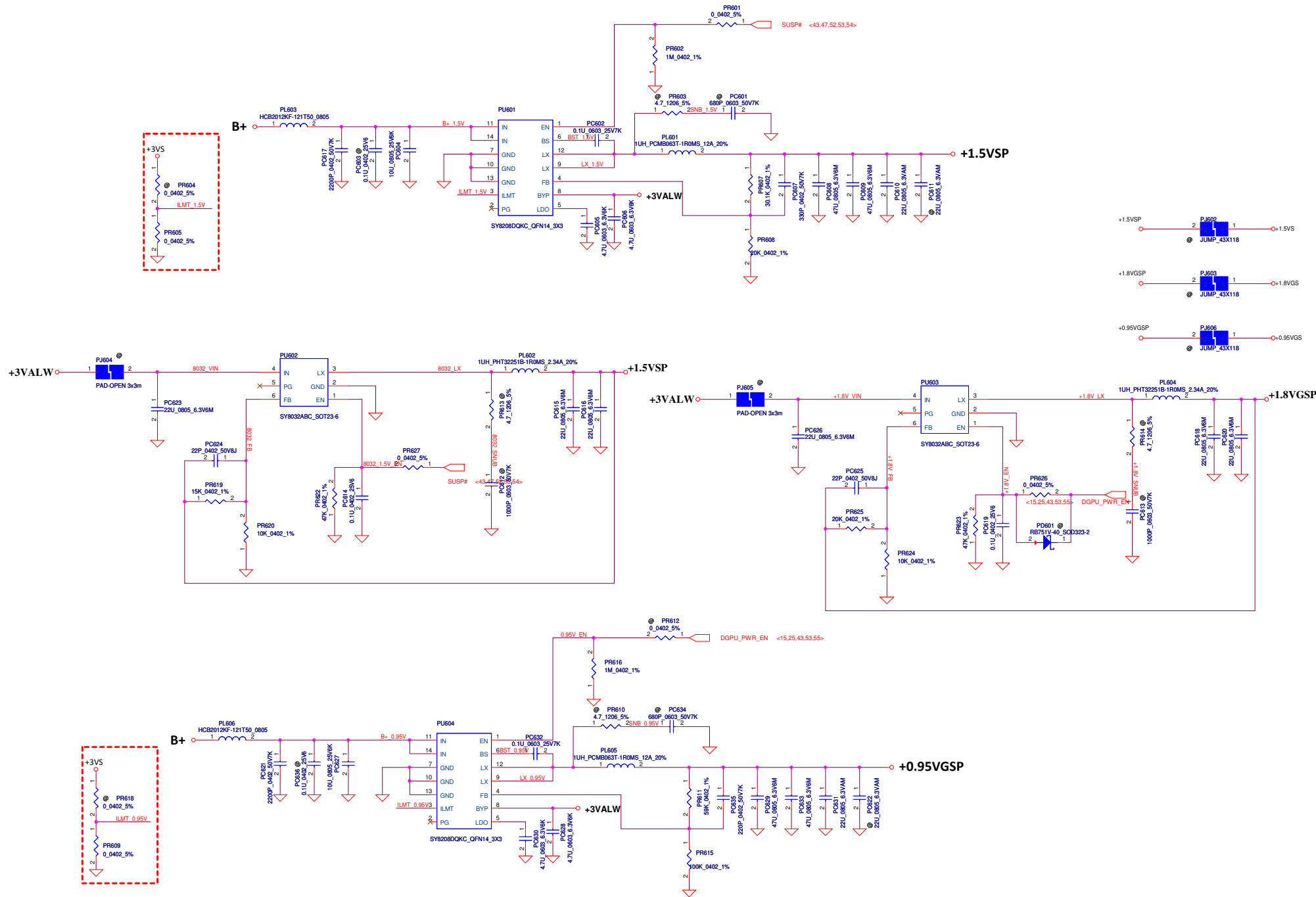
<b>Compal Electronics, Inc.</b>				
Title		PWR-BATTERY CONN/OTP		
Doc Type	Document Number			Rev
Customer	Gx00			0.1
Date:	Thursday, October 11, 2012	Sheet	49	of 59





Security Classification	Compal Secret Data			Title	
Issued Date	2011/10/03	Deciphered Date	2014/12/31	PWR-3 VALWP/5VALWP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FROD AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED, COPIED, EITHER IN WHOLE OR IN PART, OR THE INFORMATION IT CONTAINS MAY BE USED BY OR FOR SCORING TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Gx00	0.1
Date: Thursday, October 11, 2012				Sheet	51 of 12

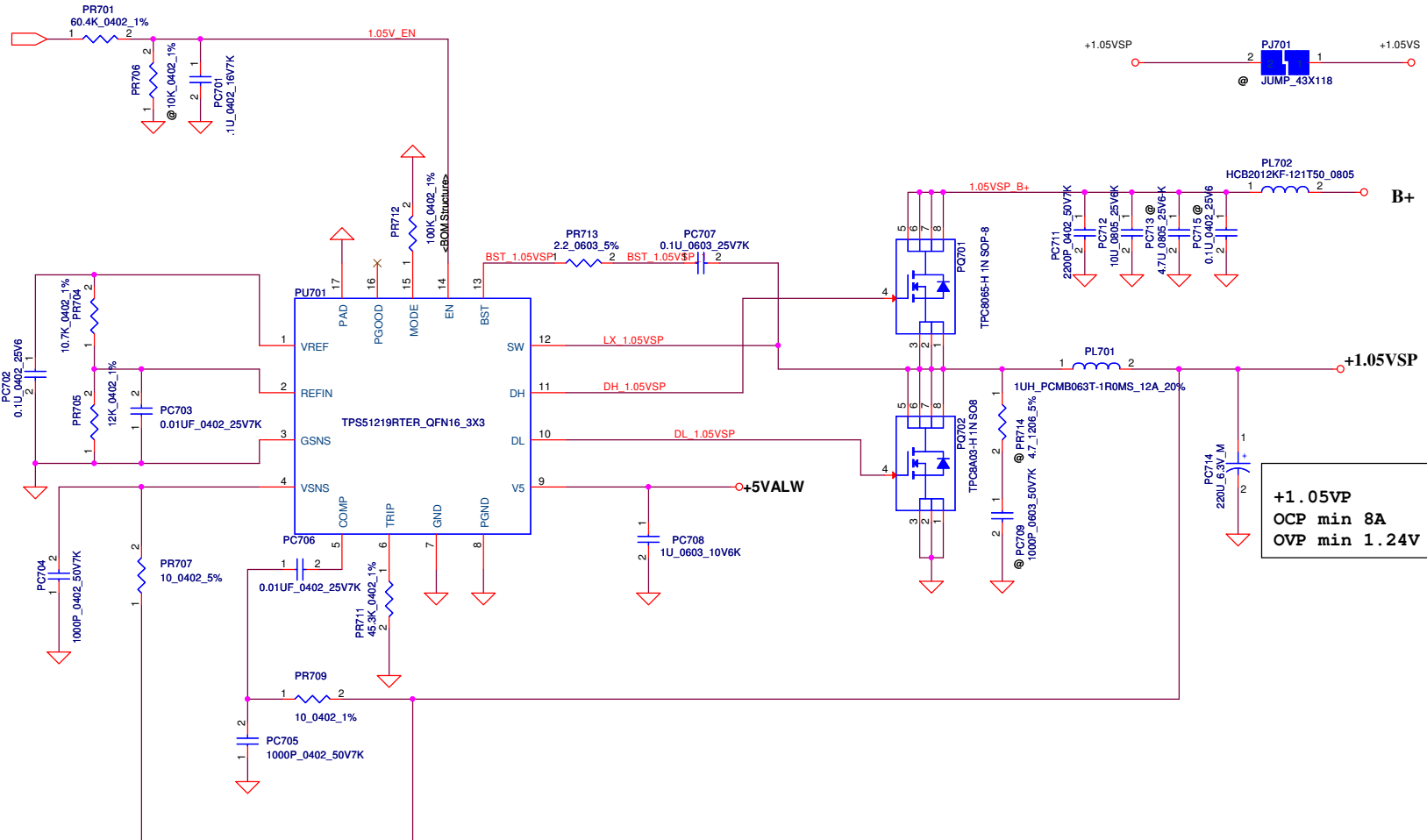




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2010/01/25		2012/07/11		1.5V_VRAM/1.8V/0.95V	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number		Rev	
Gx00		0.1		Date: Thursday, October 11, 2012	
Sheet		53		of	
59					

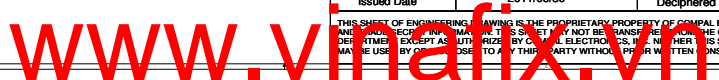
www.vmatix.vn

<43,47,52,53> SUSP#

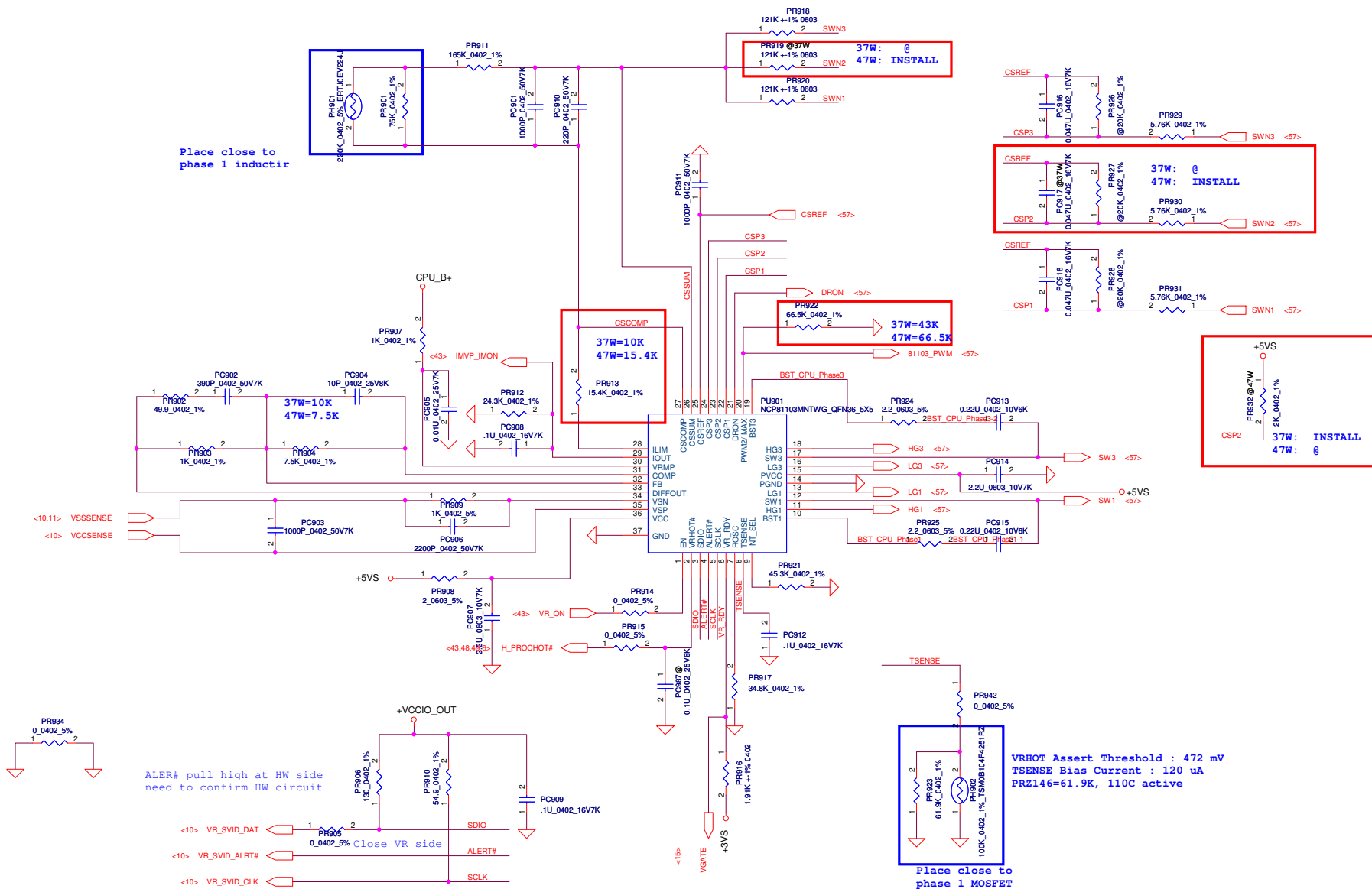


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	+1.05VS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE REPRODUCED OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number Gx00
				Date	Thursday, October 11, 2012
				Sheet	54 of 59
				Rev	0.1

www.vinallix.vn

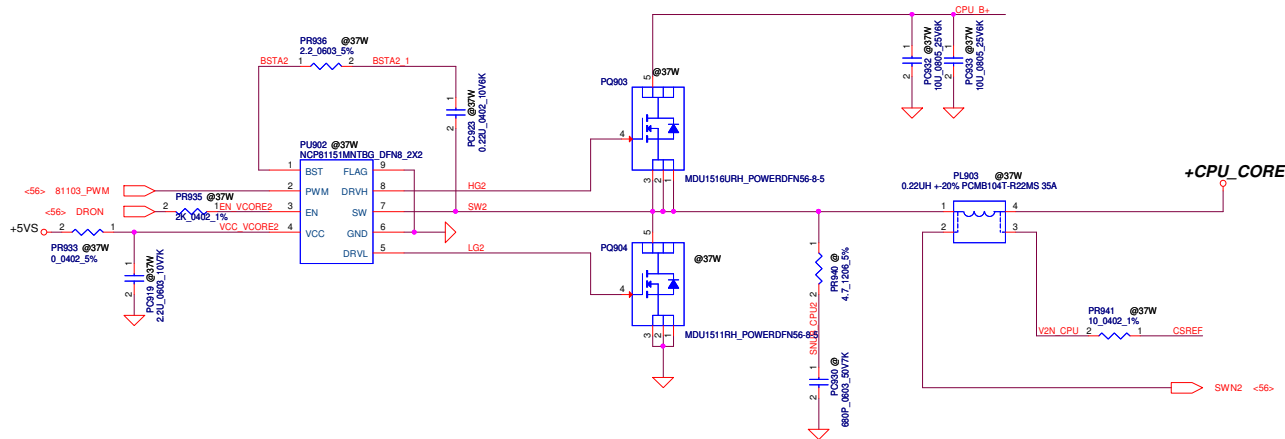
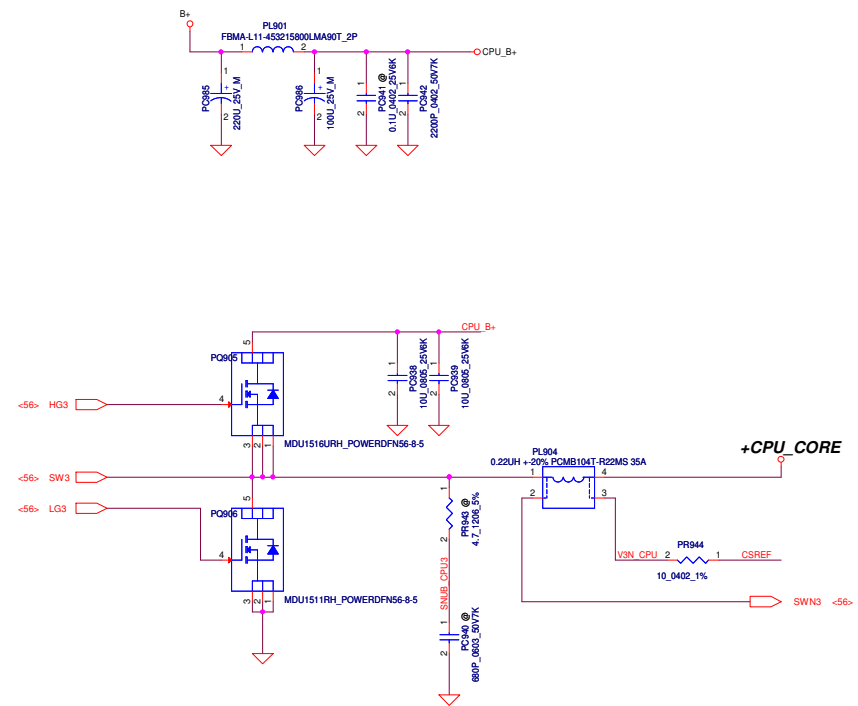
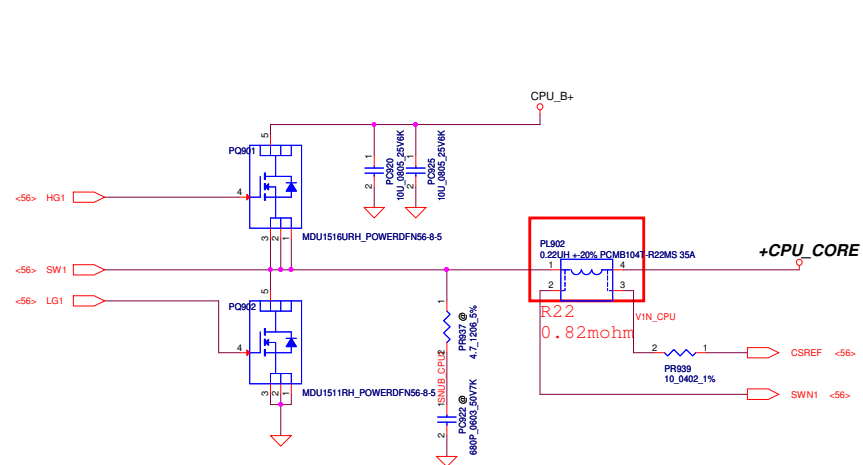


INITIAL ID	<b>Compal Electronics, Inc.</b>			
	<b>Title</b> <b>VGA_COREP</b>			
	<b>Size</b>	<b>Document Number</b> <b>Gx00</b>		<b>Rev</b> <b>1.0</b>
	<b>Date:</b>	<b>Thursday, October 11, 2012</b>	<b>Sheet</b>	<b>55 of 59</b>



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/12/14	Deciphered Date	2012/12/31	Title	CPU CORE1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Document Number	Gx00
				Rev	1.0
				Date	Thursday, October 11, 2012
				Sheet	56 of 59





Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/12/14	Deciphered Date	2012/12/31	Title
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				Gx00
				Rev 1.0
				Date: Thursday, October 11, 2012
				Sheet 57 of 59

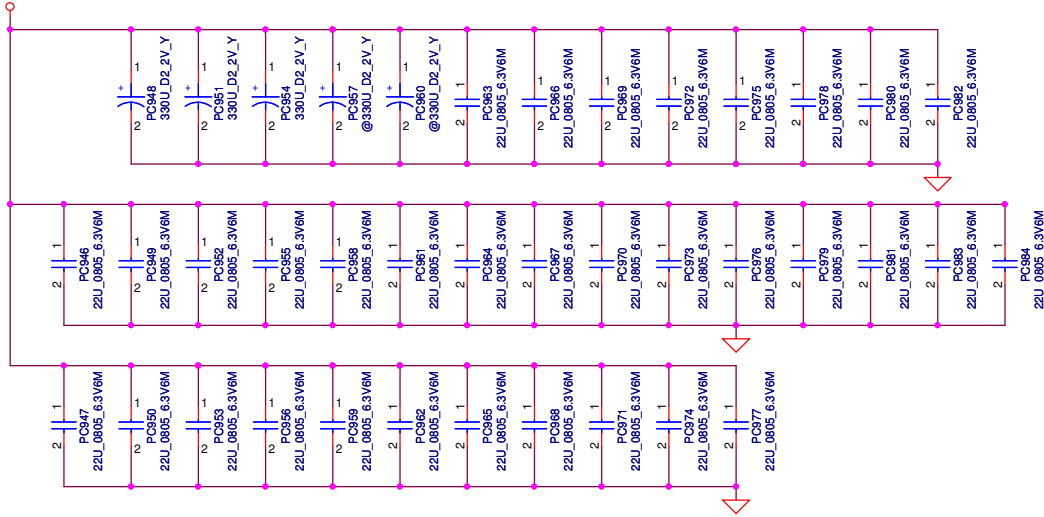
www.vimalix.vn

**+CPU\_CORE**

3 X 330u/9m (47W)  
34 X 22u/0805

2X330u/9m (37W)  
34 X 22u/0805

+CPU\_CORE



Security Classification		Compal Secret Data				Compal Electronics, Inc.								
Issued Date		2012/04/03		Deciphered Date		2014/12/31		Title						
<div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE REPRODUCED OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div>								PROCESSOR DECOUPLING						
								Size	Document Number			Rev		
								Gx00			0.1			
								Date: Thursday, October 11, 2012			Sheet 58 of 59			

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/06	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	
				Document Number Zx90	
				Rev 0.1	
Date: Thursday, October 11, 2012				Sheet 59 of 12	